I-jet guide

Rev.0.1

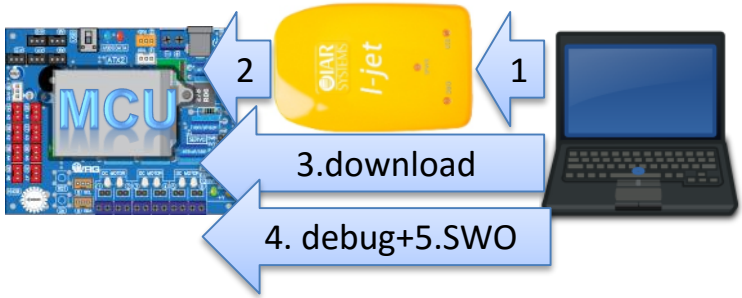
Part 1

1-1. Debugger Connection Flow

1-2. Example: Debug log

1-3. Which check list is used?

1-1. Debugger Connection Flow



1. USB connection: PC and I-jet

2. MCU Connection

3. Download to Flash(ROM)

3. Download to RAM

4. Start debug

5. SWO trace

*only for S3,S5,S7
S1 does not have SWO function

1-2. Example: Debug log(1/2)

```
Thu Jun 16, 2016 09:38:33: Loaded macro file: C:\Program Files (x86)\IAR Systems\EWARM RS-7405-11373-BETA\arm\config\debugger\Renesas\R7FS7xxxx.dmac
Thu Jun 16, 2016 09:38:34: Loading the I-jet/JTAGjet driver
Thu Jun 16, 2016 09:38:34: Probe: Probe SW module ver 1.49
Thu Jun 16, 2016 09:38:34: Probe: Option: trace(SWO,ETB)
Thu Jun 16, 2016 09:38:34: Probe: I-jet-Trace SW module ver 1.58
Thu Jun 16, 2016 09:38:34: Probe: Found I-jet, SN=72819
Thu Jun 16, 2016 09:38:34: Probe: Opened connection to I-jet:72819
Thu Jun 16, 2016 09:38:34: Probe: USB connection verified (4362 packets/sec)
Thu Jun 16, 2016 09:38:34: Probe: I-jet, FW ver 4.2, HW Ver:A
Thu Jun 16, 2016 09:38:34: Probe: None or IJET-MIPI10 adapter detected
Thu Jun 16, 2016 09:38:34: Probe: Versions: JTAG=1.65 SWO=1.34 A2D=1.62 Stream=1.41
Thu Jun 16, 2016 09:38:34: EARM v.3.81
Thu Jun 16, 2016 09:38:34: Emulation layer version 3.81
Thu Jun 16, 2016 09:38:35: SWD clock detected: 12MHz
Thu Jun 16, 2016 09:38:35: Notification to init-after-power-up hookup.
Thu Jun 16, 2016 09:38:35: Notification to core-connect hookup.
Thu Jun 16, 2016 09:38:35: Connected DAP on SWD. Detected IDCODE=0x5ba02477.
Thu Jun 16, 2016 09:38:35: CoreSight error: Debug interface power and clock request signal has not been acknowledged:
Thu Jun 16, 2016 09:38:35:          o CDBGPWRUPACK signal expected in response to assertion of CDBGPWRUPREQ.
Thu Jun 16, 2016 09:38:35:          o DAP DP STAT register is 0xd0000000.
Thu Jun 16, 2016 09:38:35:          o Debugging is not possible.
Thu Jun 16, 2016 09:38:35: CPU status FAILED
Thu Jun 16, 2016 09:38:35: Connected DAP on SWD. Detected IDCODE=0x5ba02477.
Thu Jun 16, 2016 09:38:35: Connecting on DAP AHB-AP-CM port 0 (IDR=0x24770011).
Thu Jun 16, 2016 09:38:35: Recognized CPUID=0x410fc241 Cortex-M4 r0p1 arch ARMv7-M
Thu Jun 16, 2016 09:38:35: Debug resources: 6 instruction comparators, 4 data watchpoints.
Thu Jun 16, 2016 09:38:35: CPU status - SLEEPING
Thu Jun 16, 2016 09:38:35: LowLevelReset(system, delay 200)
Thu Jun 16, 2016 09:38:35: CPU status - IN RESET
Thu Jun 16, 2016 09:38:35: CPU status OK
```

USB Connection

MCU Connection

next Page

1-2. Example: Debug log(2/2)

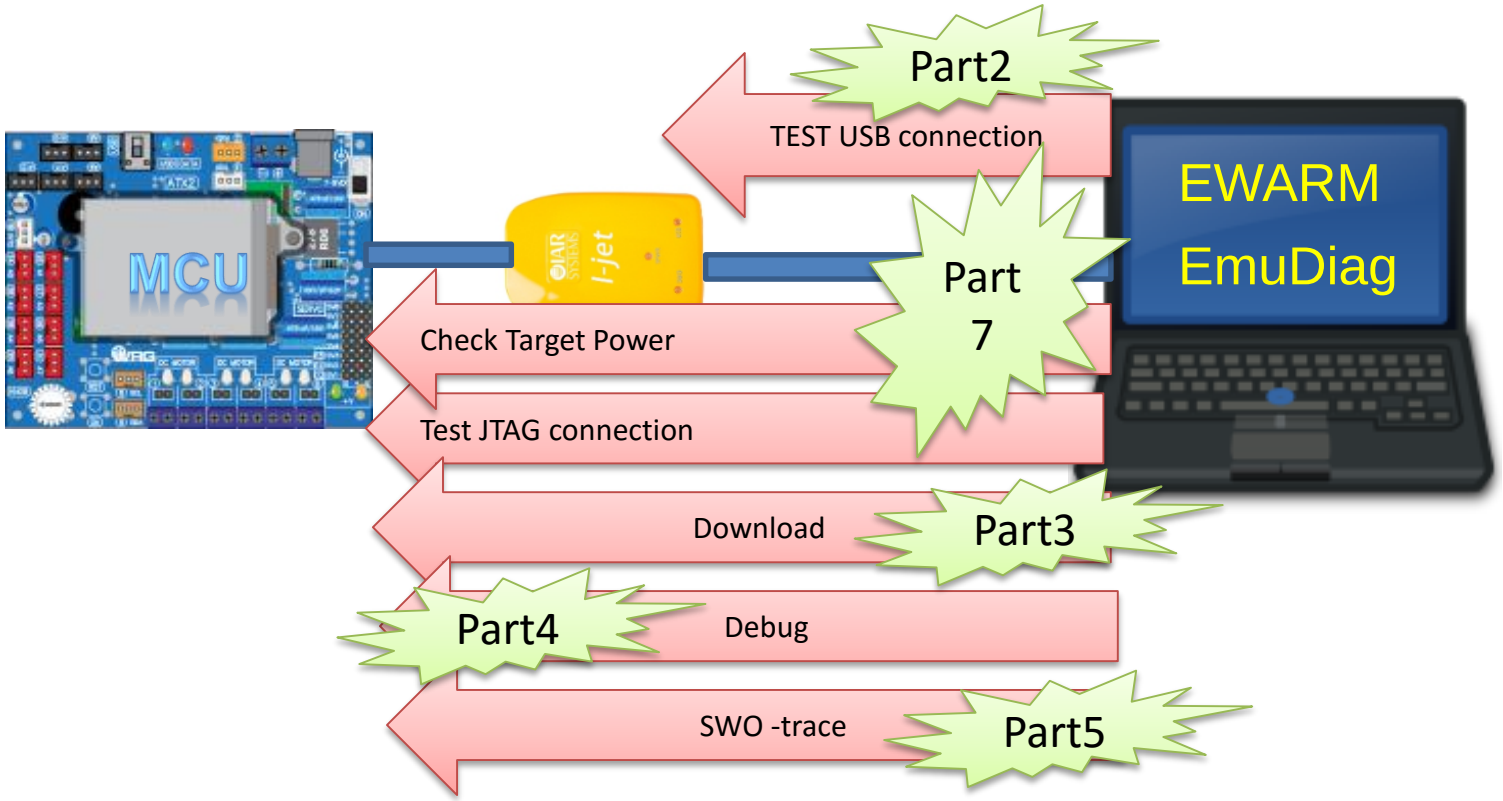
```
Thu Jun 16, 2016 09:38:36: Loaded debugee: C:\Program Files (x86)\IAR Systems\EWARM RS-7405-11373-
BETA\arm\config\flashloader\Renesas\FlashR7FS7G2x640K.out
Thu Jun 16, 2016 09:38:36: Target reset
Thu Jun 16, 2016 09:38:40: Skipping flash loading pass because there is no data in the designated range: 0x40100000-0x4010FFFF.
Thu Jun 16, 2016 09:38:40: Downloaded C:\Users\HirokiAk\Desktop\Renesas SSP training_Japan\EWSYN_Hands-
On\lab4_migration\WeatherPanel\Debug\Exe\lab4.out to
flash memory.
Thu Jun 16, 2016 09:38:49: Loaded debugee: C:\Users\HirokiAk\Desktop\Renesas SSP training_Japan\EWSYN_Hands-
On\lab4_migration\WeatherPanel\Debug\Exe\lab4.out
Thu Jun 16, 2016 09:38:50: LowLevelReset(software, delay 200)
Thu Jun 16, 2016 09:38:50: LowLevelReset(system, delay 200)
Thu Jun 16, 2016 09:38:50: CPU status - IN RESET
Thu Jun 16, 2016 09:38:50: CPU status OK
Thu Jun 16, 2016 09:38:50: 593504 bytes downloaded into FLASH and verified (102.08 Kbytes/sec)
Thu Jun 16, 2016 09:38:50: Download completed and verification successful.
Thu Jun 16, 2016 09:38:50: LowLevelReset(software, delay 200)
Thu Jun 16, 2016 09:38:50: Target reset
Thu Jun 16, 2016 09:38:50: INFO: Configuring trace using 'SWO,ETB' setting ...
Thu Jun 16, 2016 09:38:50: ETB, ID:0x00000021, Capacity:2KB (2K samples)
Thu Jun 16, 2016 09:38:50: SWO: Manchester, Pin = TDO, CPU clock = 72000kHz, Auto divider = 4
Thu Jun 16, 2016 09:38:50: INFO: Cannot measure current when I-jet is not powering the target.
Thu Jun 16, 2016 09:38:54: There was 1 warning during the initialization of the debugging session.
```

Download (FLASH)

Start Debug

* this is one example of Debug log

1-3. Which check list is used?



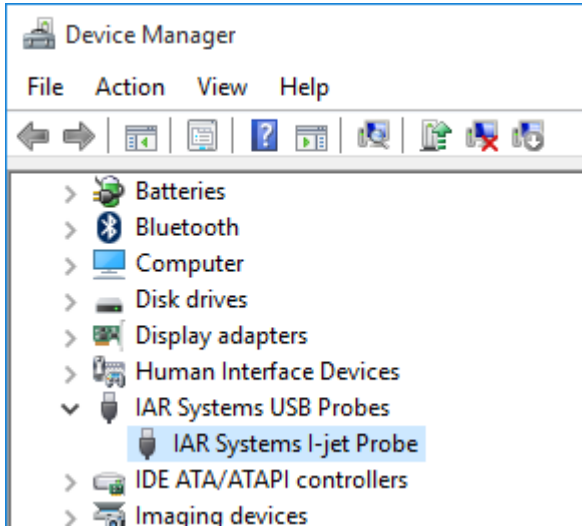
Part 2

- This is a check list when you cannot connect to MCU.

2-1. Does Host PC recognize your I-jet(Hardware debugger)?
2-2. Test Connection to I-jet
2-3. Check your Connection
2-4. Check JTAG/SWD interface
2-5. Debug port cannot be used for other purpose
2-6. check cable and connector
2-7. Check the driver: I-jet/JTAGjet
2-8. Check Power Supply to board
2-9. Check Connection Speed
2-10. Check I-jet Indicators

2-1. Does Host PC recognize your I-jet(Hardware debugger)?

- Check “Device Manager” in Windows OS



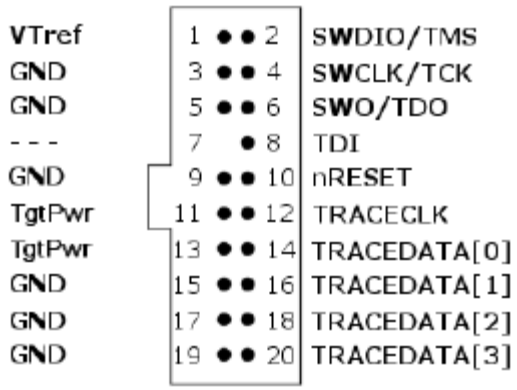
2-2. Test Connection to I-jet

- EmuDiag is the tool to check the connection
- -> Part 7

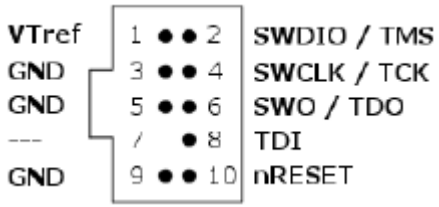
2-3. Check your Connection(1)

- There are several hardware interface:
- MIPI-20, MIPI-10, ARM-20

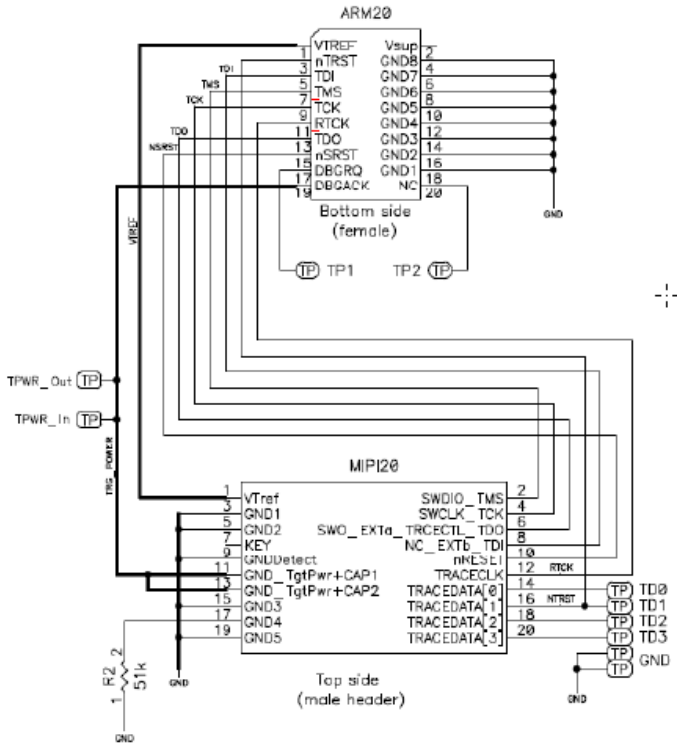
- Be sure which type is using!



JTAG/SWD - MIPI-20



JTAG/SWD - MIPI-10



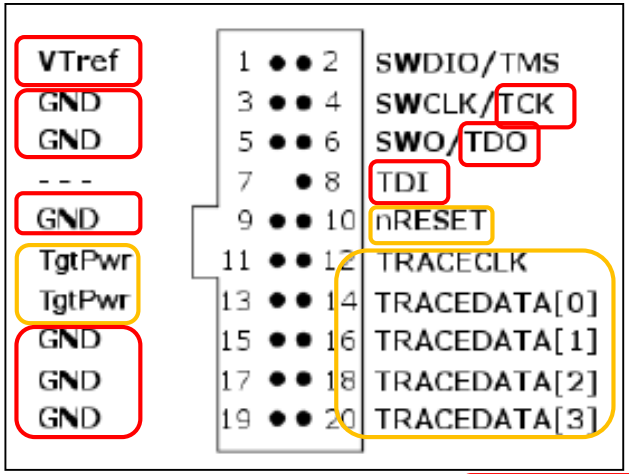
MIPI-20 - ARM-20 JTAG Adaptor

IAR Embedded Workbench for Synergy has document,
“IAR Debug probes User Guide I-jet, I-jet Trace, and I-scope”

2-3. Check your Connection(2)

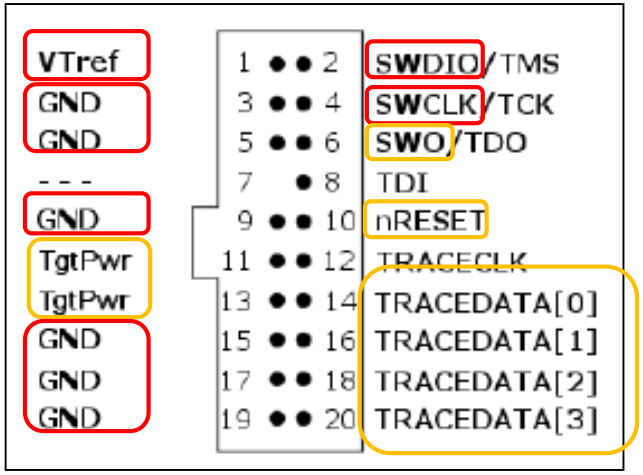
- Connection to VTref is indispensable.
  VTref is to check whether the target has power,
  to create the logic-level reference for the input comparators, and
  to control the output logic levels to the target.
- All GND pins should be connected.
  - Less connections tends unstable.

JTAG interface



mandatory

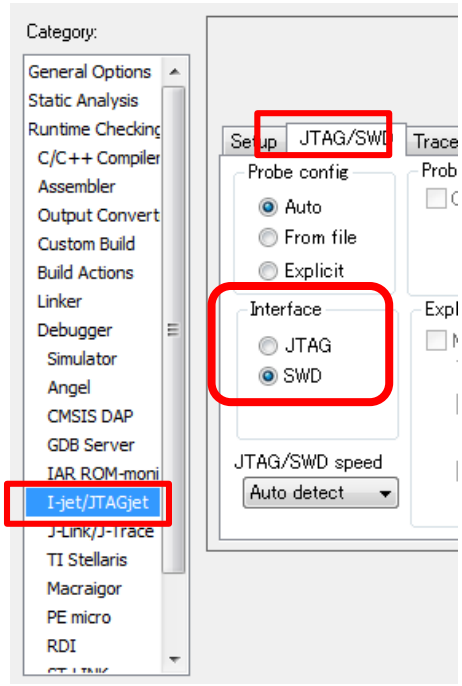
SWD interface



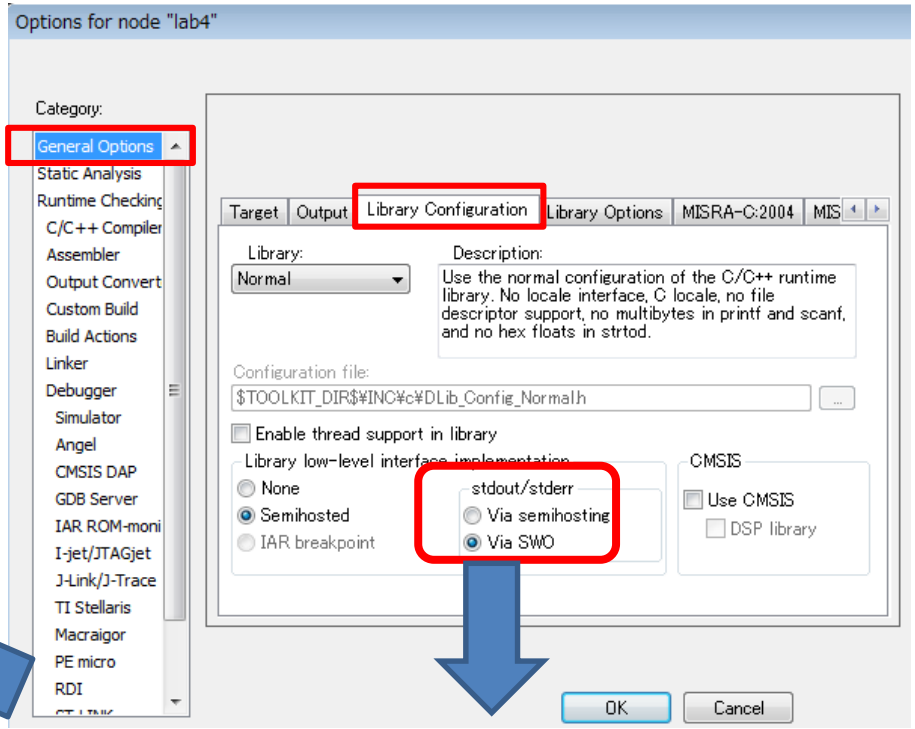
option

2-4. Check JTAG/SWD interface

In Project option, interface must be selected JTAG or SWD.



S3,S5 and S7 can select JTAG or SWD.
S1 supports only SWD.



S3,S5, S7, can select semihosting or SWO.
If SWO is selected, JTAG interface cannot be selected.

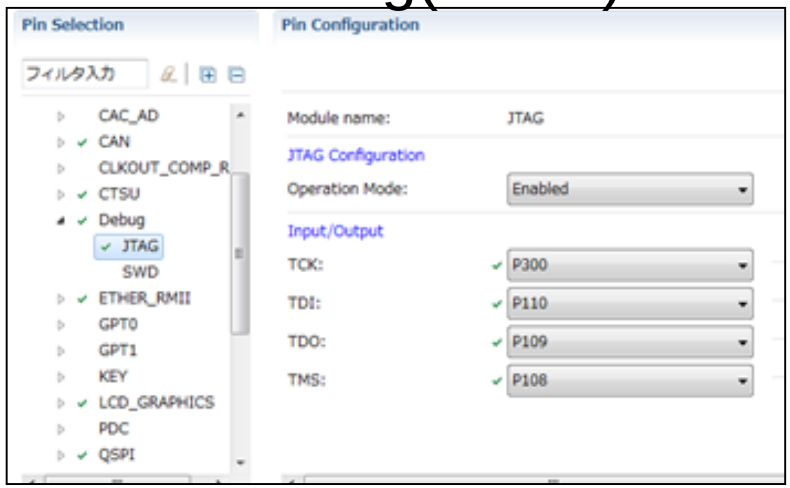
S1 does not support SWO..

2-5. Debug port cannot be used for other purpose

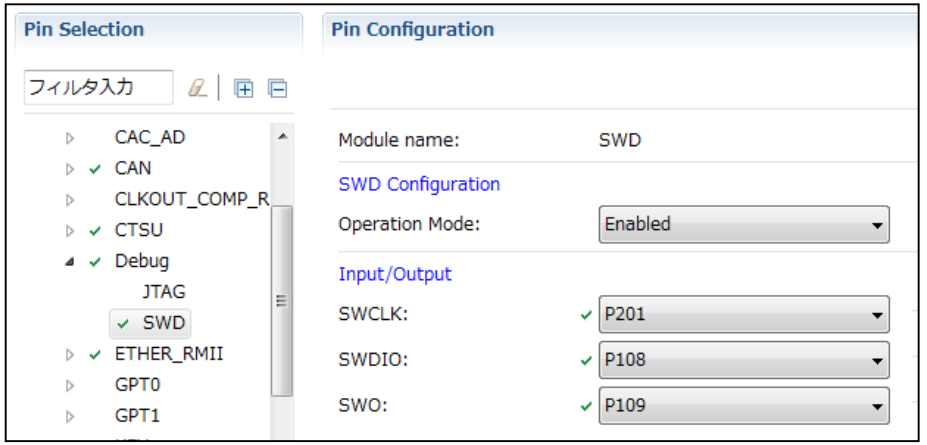
- JTAG/SWD port can be used for other purpose.
  Synergy S1's case:
  SWCLK is shared with P300, GTOUUP_C, GTIOC0A and SSLB1_B.
- Don't use debug port for other purpose when debugging.

Synergy Standalone Configurator

JTAG setting(S7G2)



SWD setting(S7G2)



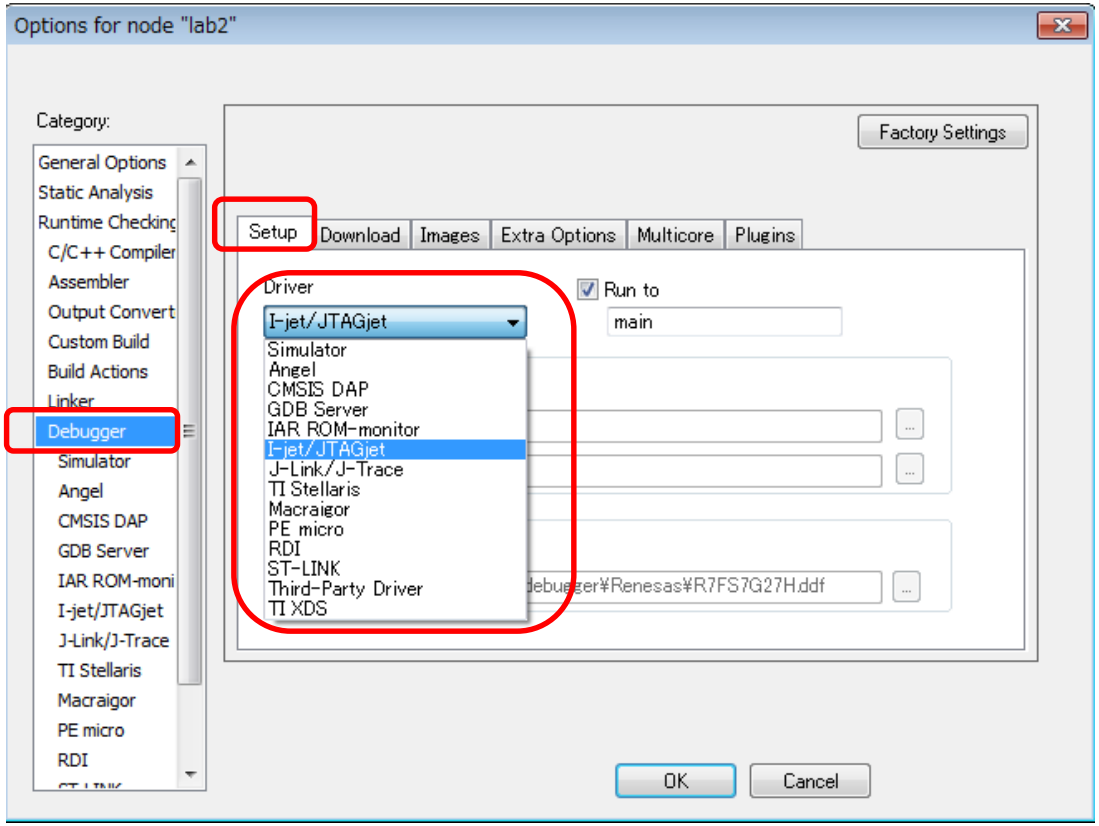
2-6. check cable and connector

- Do connector and cable have anything damaged?
- Check Looseness of cable/ contact failure
- Check direction of connector

- if possible, try new USB cable/ FLAT cable

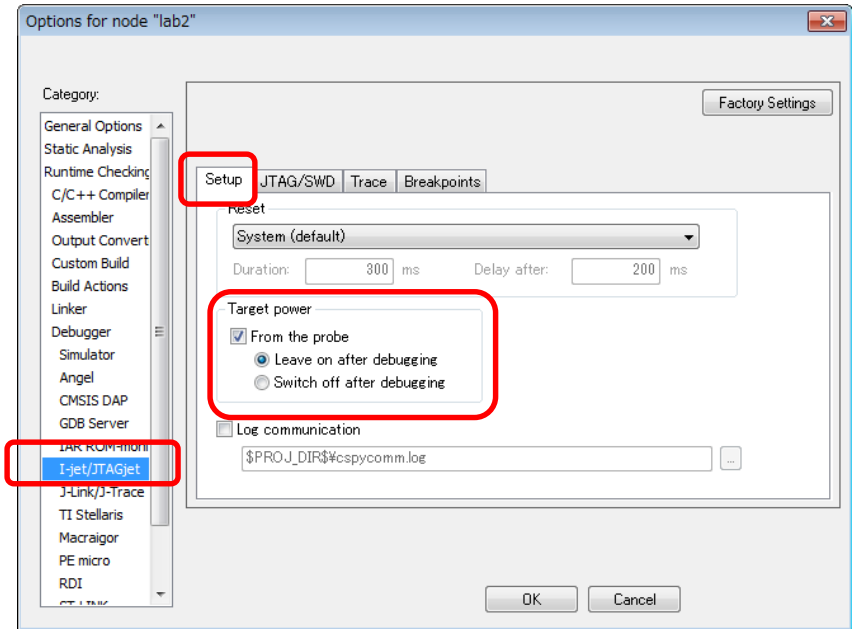
2-7. Check the driver: I-jet/JTAGjet

- Check the driver in debugger option,
- [I-jet/JTAGjet] should be selected.



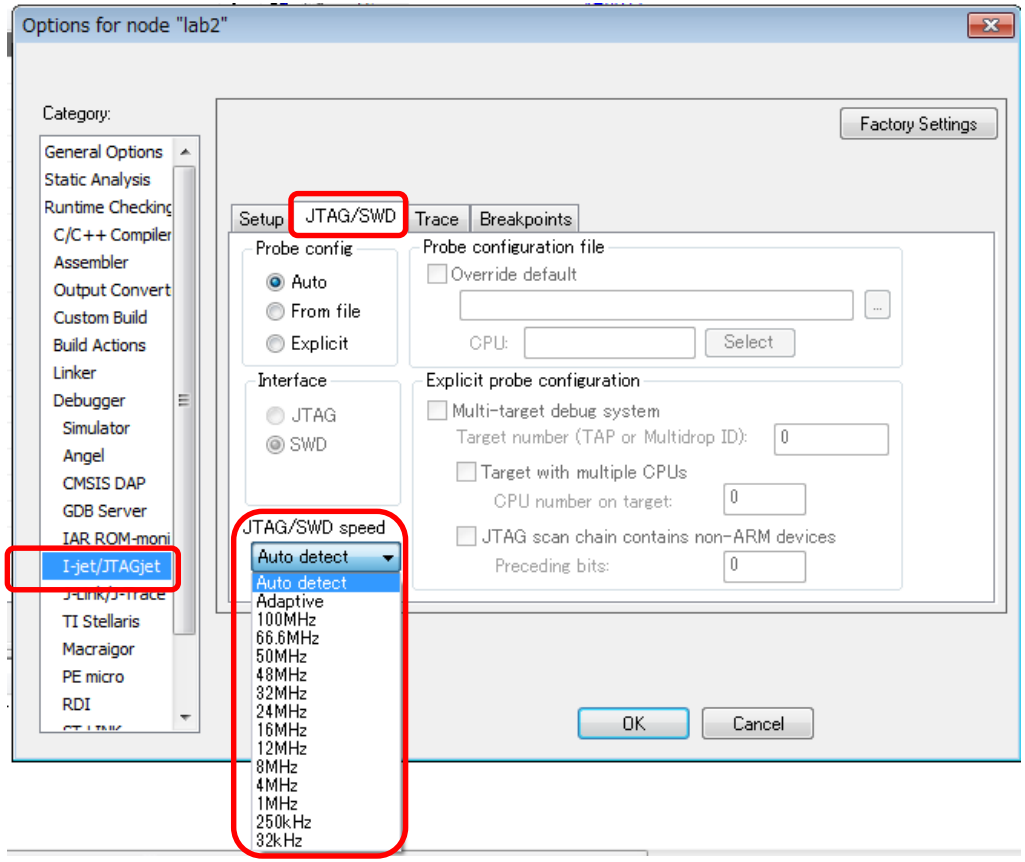
2-8. Check Power Supply to board

- How to supply power ?
  - from ICE probe, or USB or external Power supply
- From ICE probe, option should be checked.



2-9. Check Connection Speed

- Try slow JTAG/SWD speed, for example, 1MHz or 250KHz
- JTAG/SWD speed depends on PCB/Circuit design, connector, cable …



2-10. Check I-jet Indicators

The TPWR indicator (Target power)

Indicator status	Description
Off	Power to target is not provided by I-jet.
Green	Power to target is provided by I-jet.
Yellow	Warning. Power to target is above 420 mA.
Red	Error. Overcurrent limit (520 mA) detected and power to target was switched off for protection.

The DBG indicator (JTAG/SWD)

Indicator status	Description
Off	vTRef on JTAG header is too low.
Green	vTRef is at or above 1.8 V.
Green blinking	Indicates JTAG/SWD communication activity.

The USB indicator

Indicator status	Description
Off	No USB power.
Green steady	Initial state or no transfer.
Green blinking	USB transfers to or from I-jet.
Red blinking	USB enumeration.
Red steady	USB did not enumerate or broken hardware.

Part 3

- How to check Download trouble?

3.1 Check matching of Linker Setting File

3-2. Check download option setting

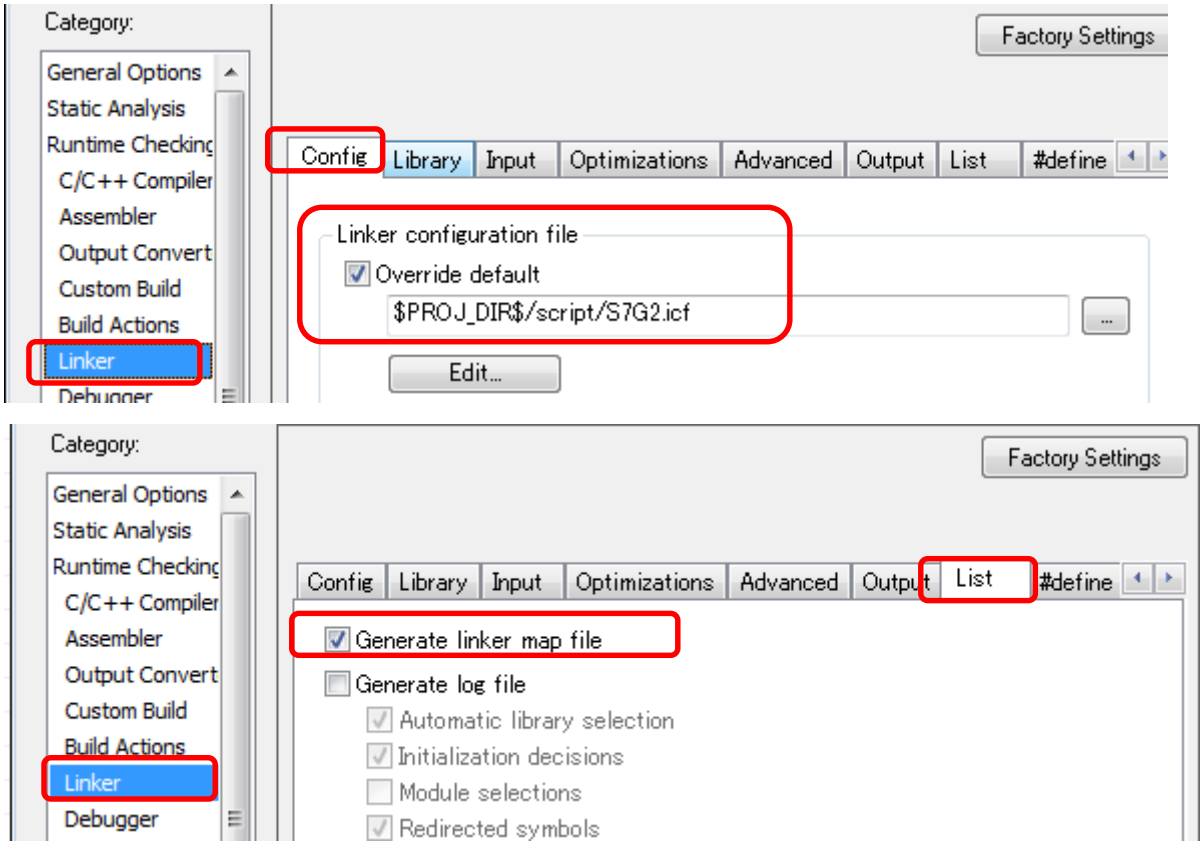
3-3. Check reset strategy for your board

3-4. check download to RAM

3-5. Check JTAG/SWD speed

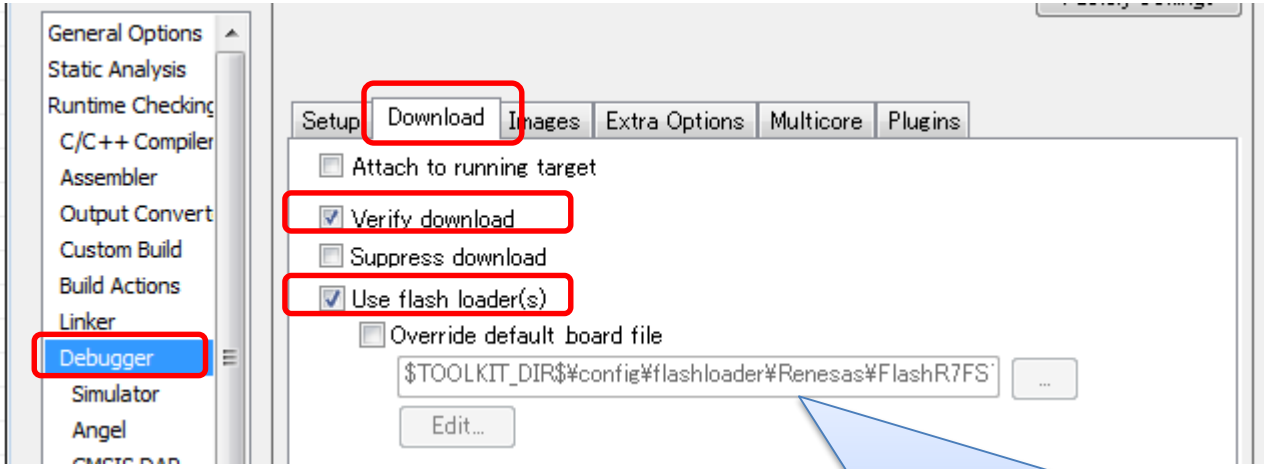
3.1 Check matching of Linker Setting File

- Check all data are is in download memory region.
  ⇒check linker setting file and map file.



3-2. Check download option setting

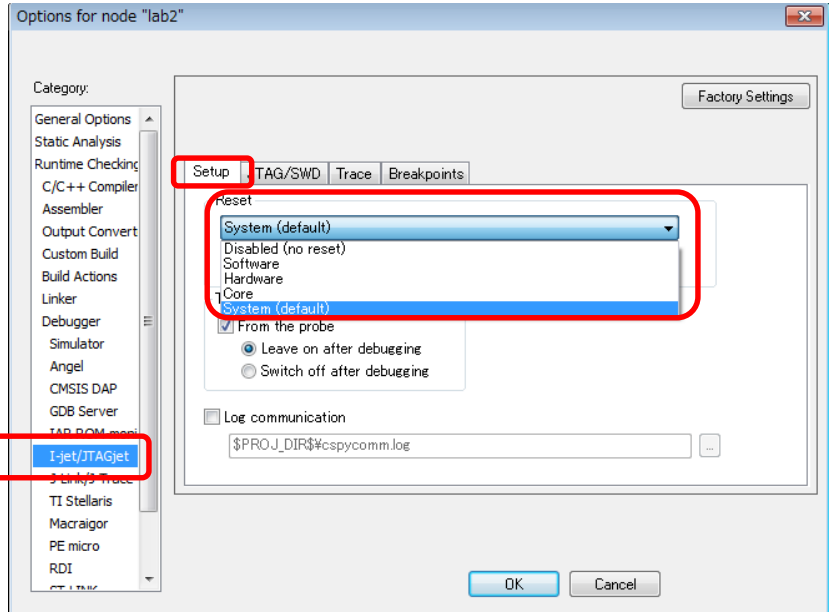
- Check [Use flash loader] is enabled.
- Customized Flashloader is required to download FLASH(ROM) region.



EW for Synergy includes Flashloaders for internal FLASH of Synergy MCUs.

3-3. Check reset strategy for your board

- Please select right reset strategy.



Disabled(no reset) : No reset is performed.

Software : Sets PC to the program entry address and SP to the initial stack pointer value.

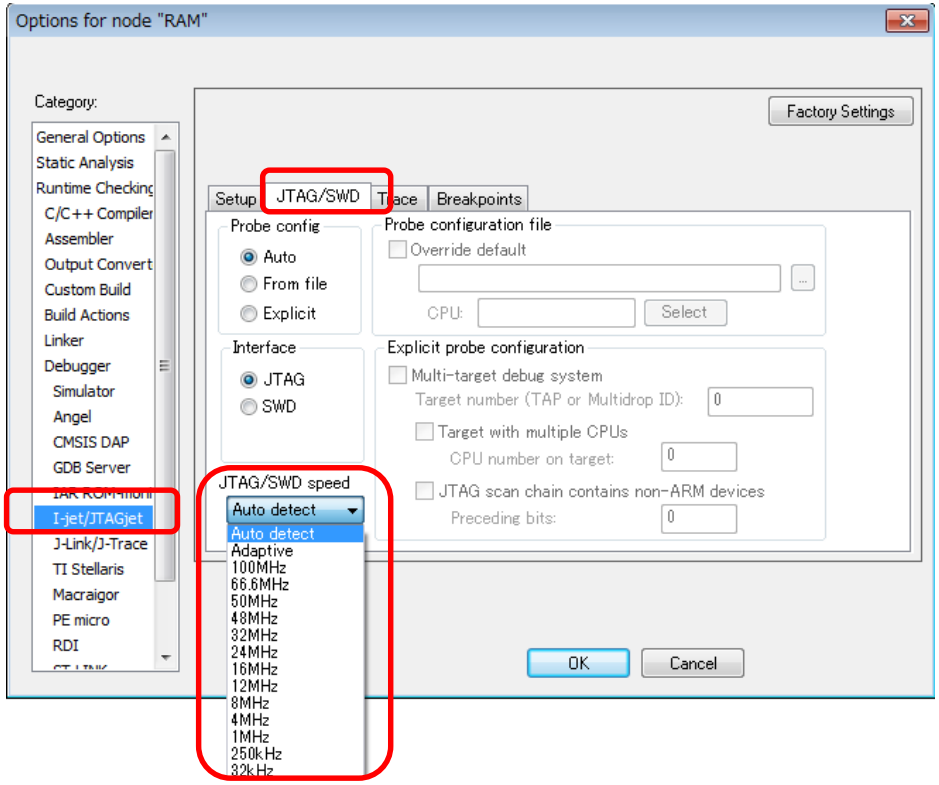
Hardware : The probe toggles the nSRST/nRESET line on the JTAG connector to reset the device.

Core : Resets the core via the VECTRESET bit; the peripheral units are not affected.

Systems (default) : Resets the core and peripheral units by setting the SYSRESETREQ bit in the AIRCR register

3-5. Check JTAG/SWD speed

- Download needs more stable than JTAG/SWD connection.
- When download has problem, try to select lower speed.



Part 4

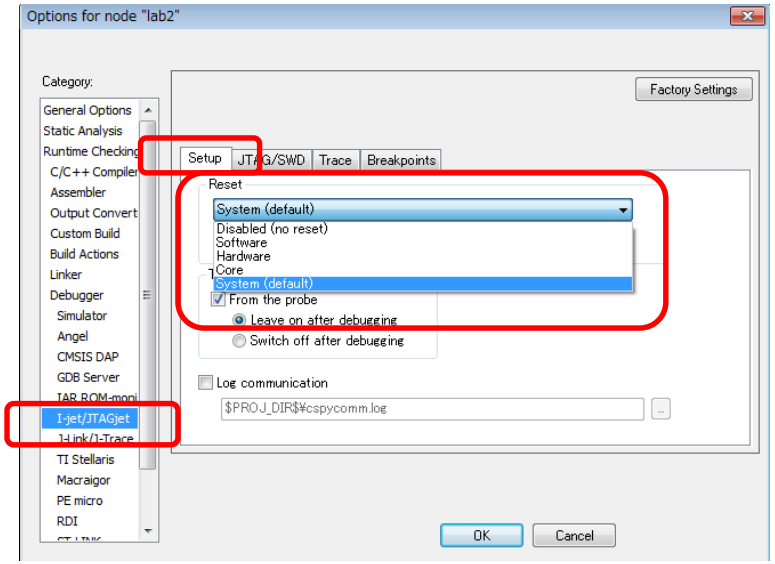
- What should be checked in the case you cannot debug

4-1. Check reset strategy for your board

4-2. Check starup code!

4-1. Check reset strategy for your board

- Please select right reset strategy.



Disabled(no reset) : No reset is performed.

Software : Sets PC to the program entry address and SP to the initial stack pointer value.

Hardware : The probe toggles the nSRST/nRESET line on the JTAG connector to reset the device.

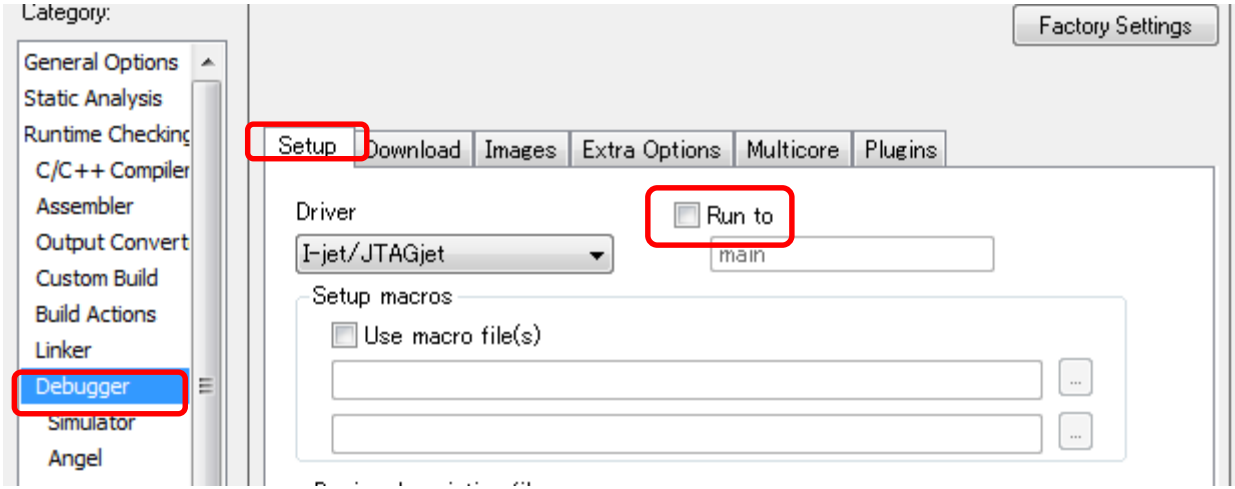
Core : Resets the core via the VECTRESET bit; the peripheral units are not affected.

Systems (default) : Resets the core and peripheral units by setting the SYSRESETREQ bit in the AIRCR register

4-2. Check starup code!

- When a program does not stop at main function, after target program is downloaded without trouble, check startup code step by step.

[Debug]→[Setup]→disable [Run to] main



Part 5

- What should be checked in the case you cannot get SWO trace.

5-1. Check SWD interface is selected

5-2. check SWO connection

5-3. Check SWO protocol

5-4. Check trace function is enabled

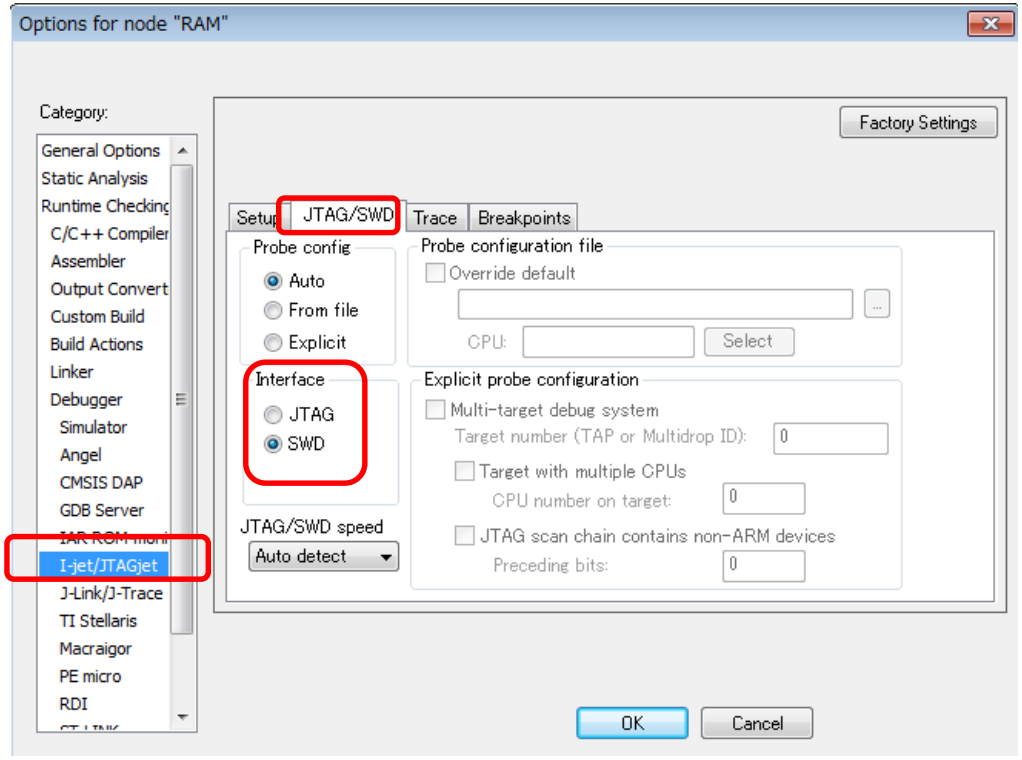
5-5. SWO trace has limited bandwidth

---

* S1 does not support SWO.

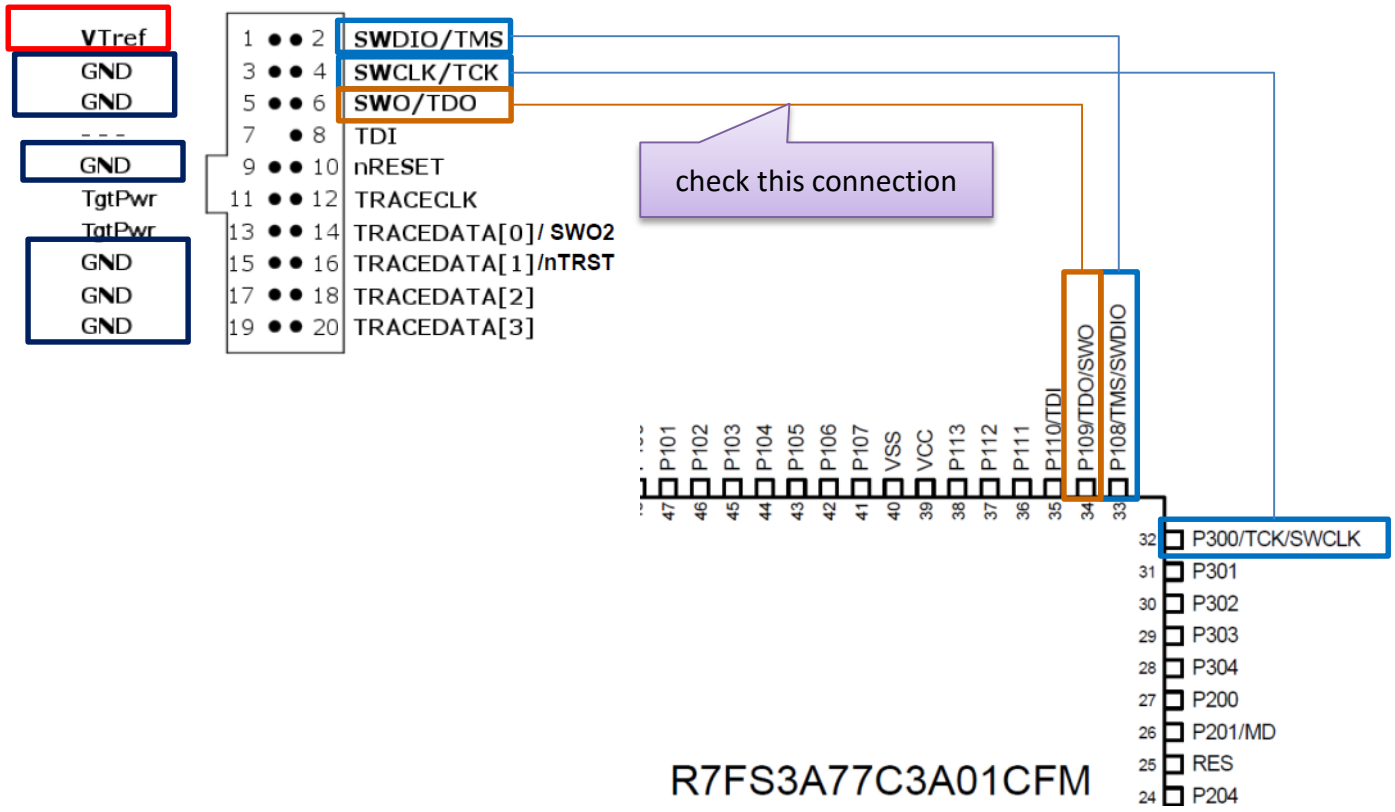
5-1. Check SWD interface is selected

- SWD connection must be selected for SWO trace [I-jet/JTAGjet]-[JTAG/SWD]-Interface [SWD]



5-2. check SWO connection

- Confirm that SWO pin of MCU is connected to connector of I-jet.



5-3. Check SWO protocol

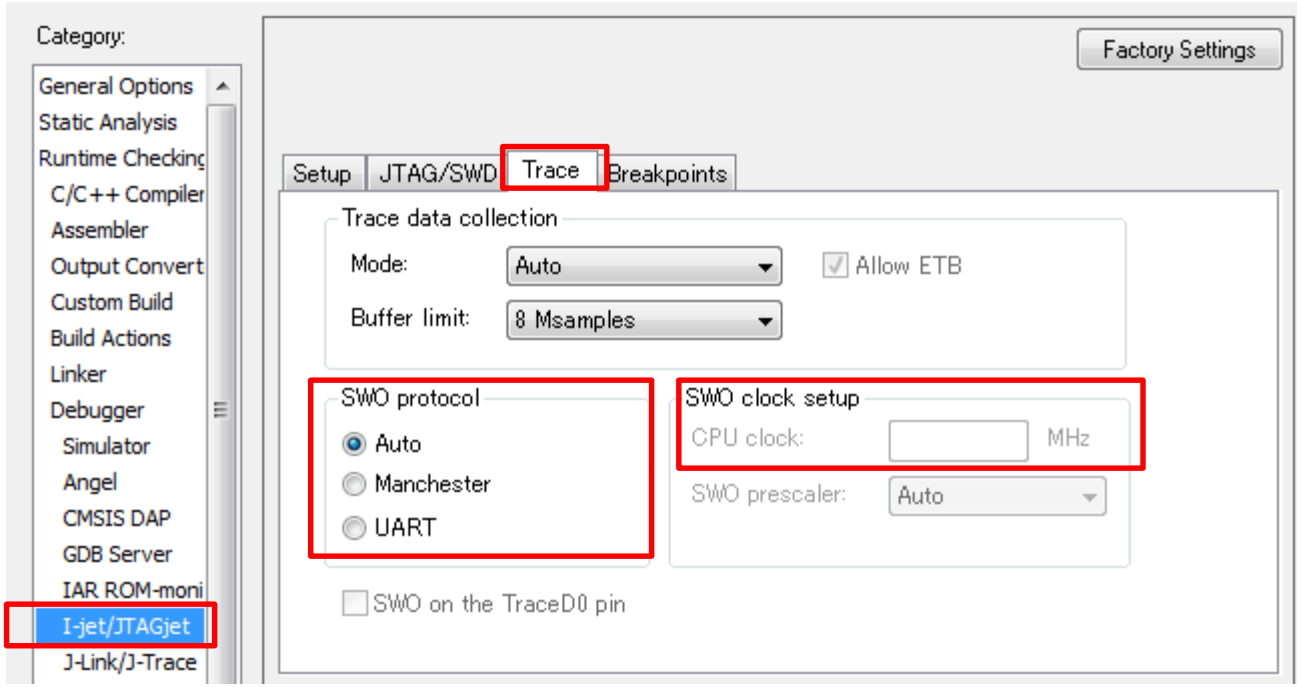
- SWO trace needs clock seting

[I-jet/JTAGjet]-[Trace]-[SWO protocol],

1st: Try “Auto” setting

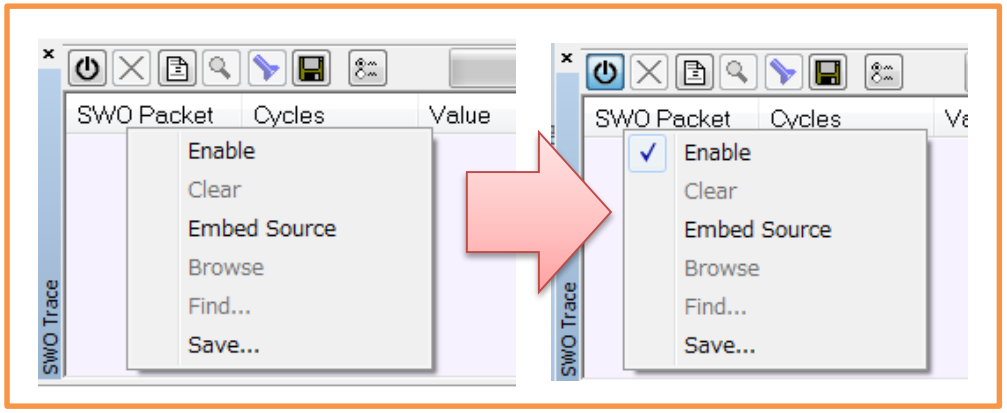
2nd: Try “Manchester” setting

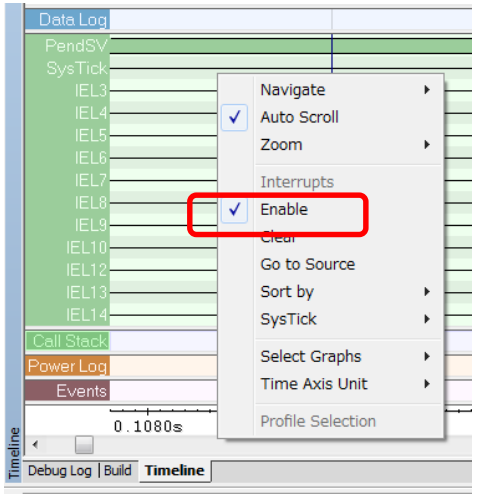
3rd: Select “UART” and set [CPU clock]



5-4. Check trace function is enabled

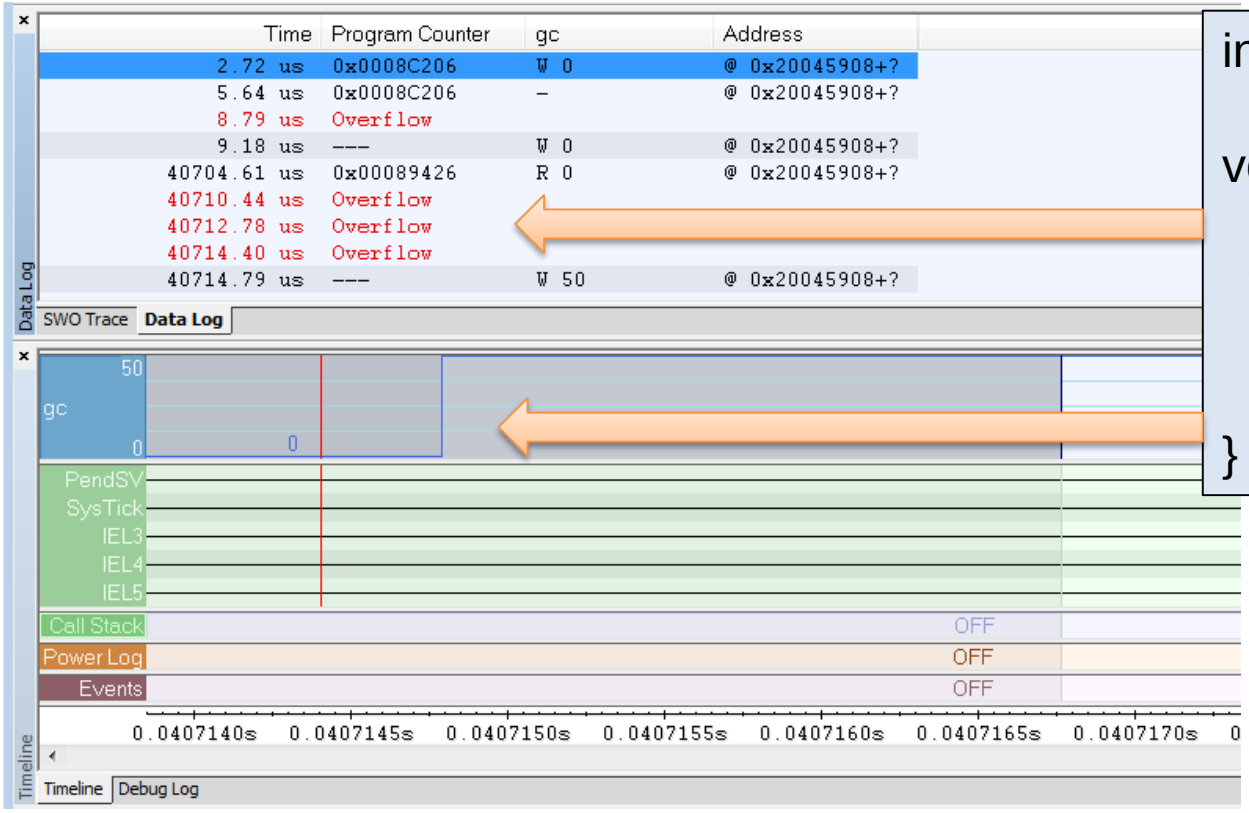
- Each trace function needs to enable it for getting data





5-5. SWO trace has limited bandwidth

- If the output data is too much,
  trace data may be lost due to an overflow.




```
int   gc;

void foo( void ) {
  int i;
  for (i=0; i<AAA; i++ )  {
     gc++;
  }
}
```

Part 6

Memory Configuration

6-1. What is [Memory Configuration] in I-jet/JTAGjet

6-2. Device Description File has memory configuration information

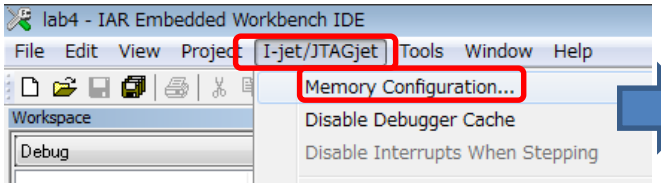
6-3. Memory Configuration can be Customized

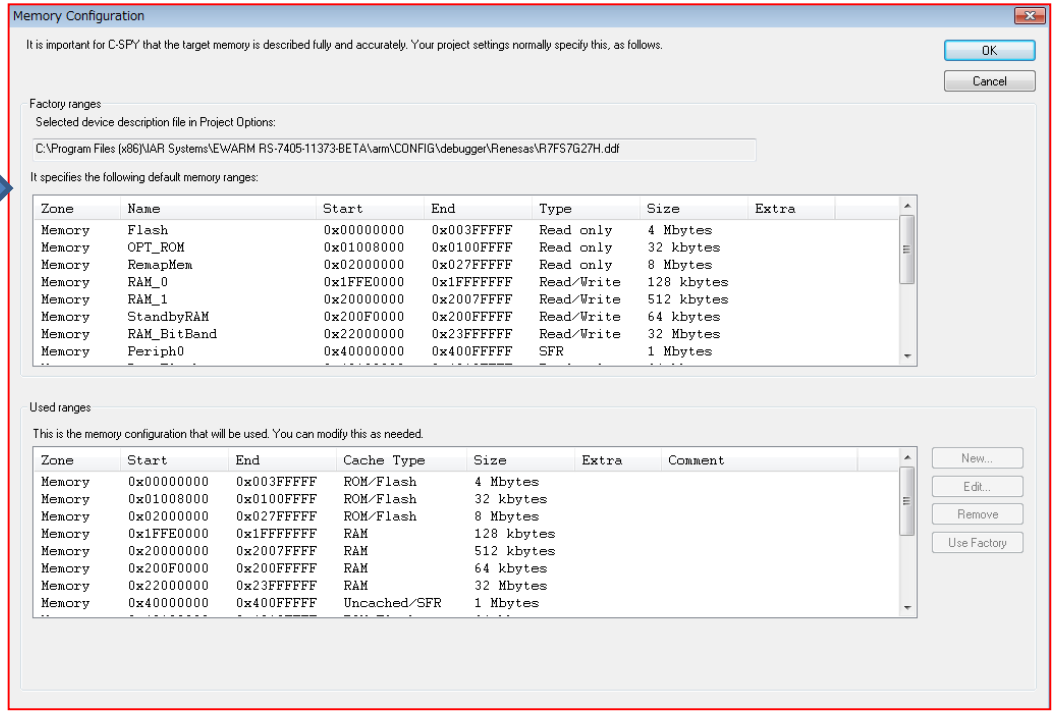
6-4. What is cache type?

6-5. What is Zone?

6-1. What is [Memory Configuration] in I-jet/JTAGjet

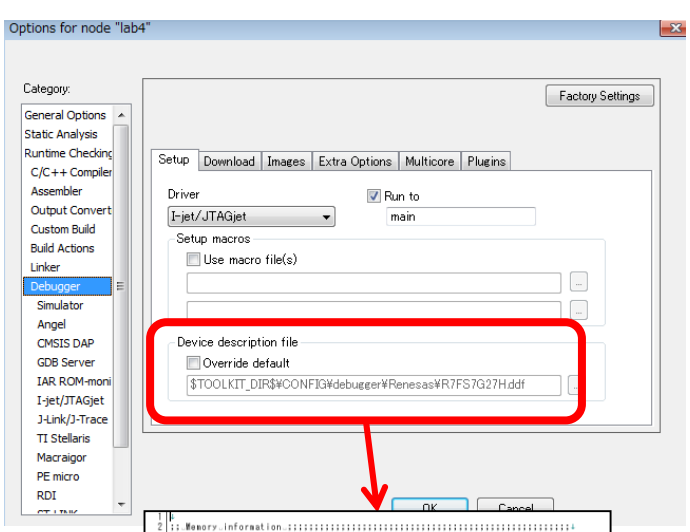
- Memory Configuration protects unintended memory access and improve debug performance.

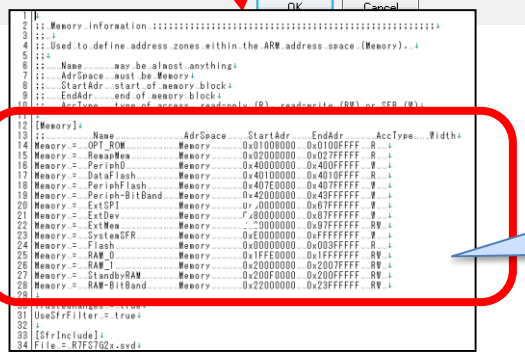




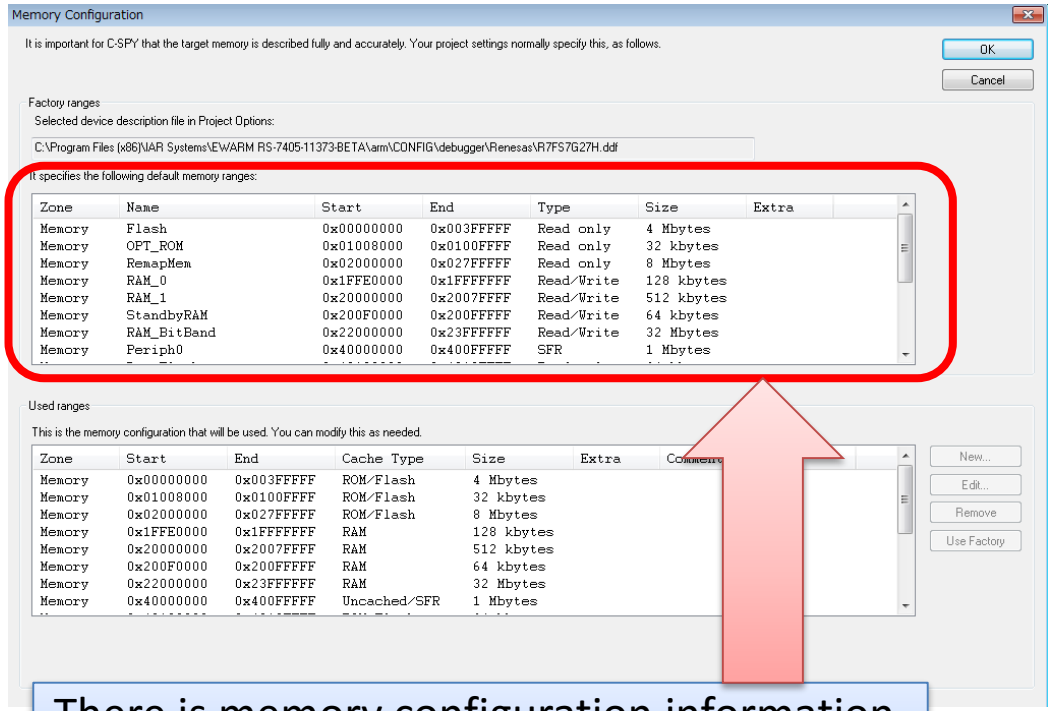
6-2. Device Description File has memory configuration information

- Project option specify the device description file which has memory configuration informaion.





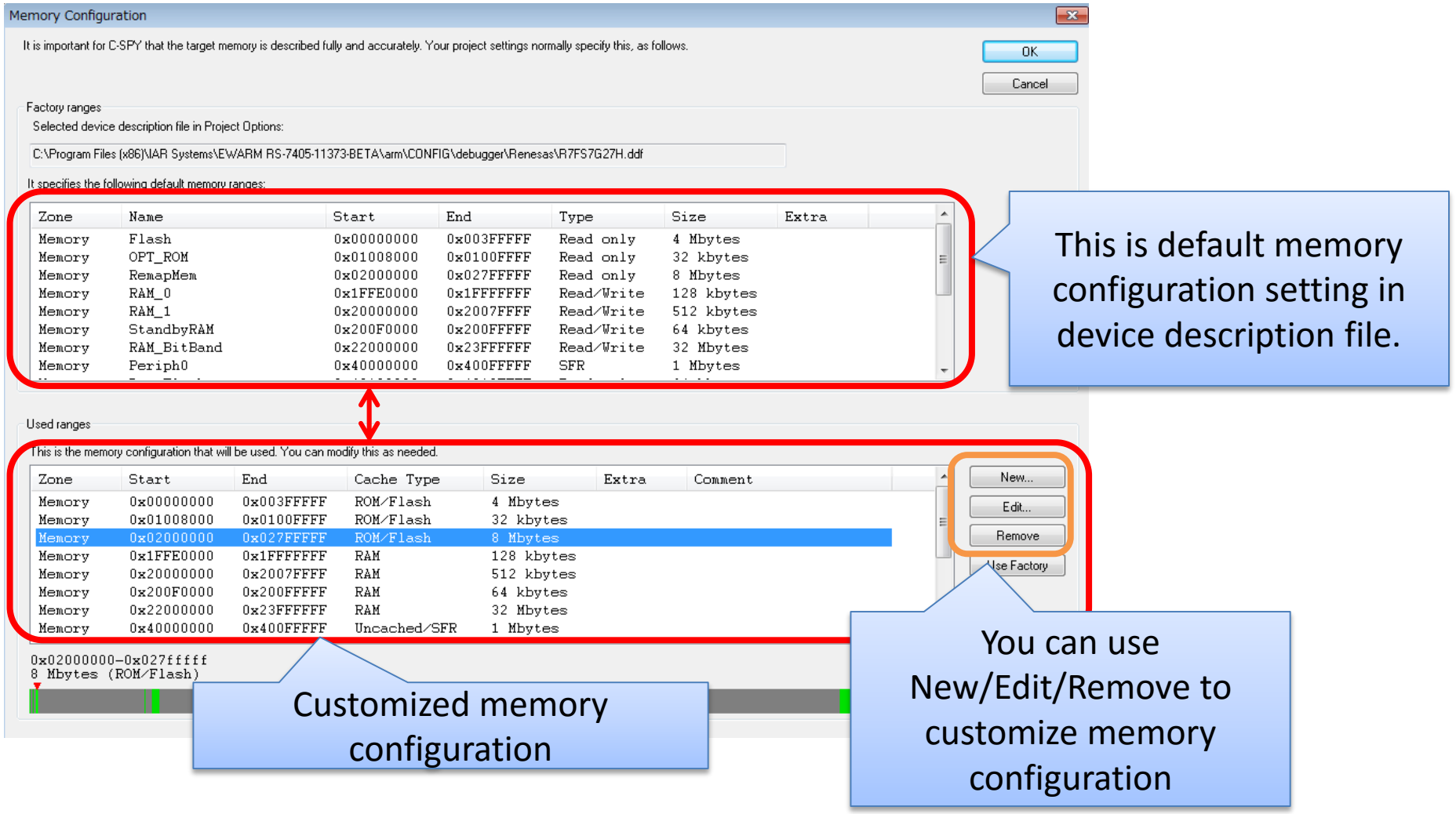
Device Description file



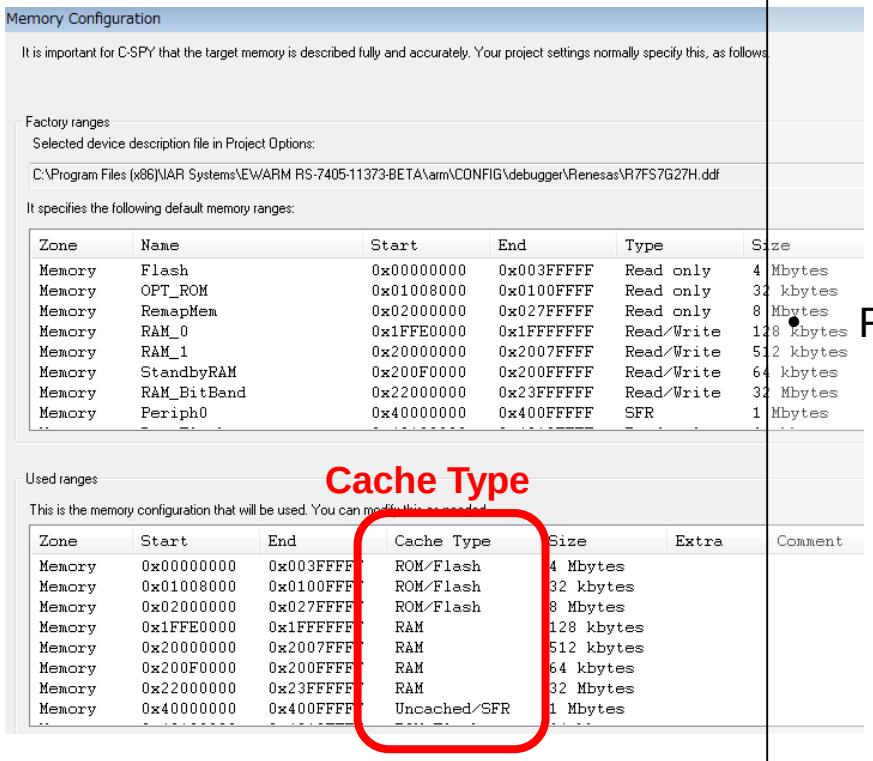
There is memory configuration information. This information is used “default memory configuration”.

6-3. Memory Configuration can be Customized

* If you use external memory , memory configuration should be customized



6-4. What is cache type?



- RAM
  When the target CPU is not executing, all read accesses from memory are loaded into the cache.
  Before any target execution, all modified bytes are written to the memory on your hardware.

- ROM/Flash
  This memory is assumed not to change during a debug session. Any code within ROM/Flash remains is stored in the cache and remains there.
  The part of flash memory which is used for a file system orsimply to store non-volatile information should designate those parts of flash memory as one or more RAM ranges instead.

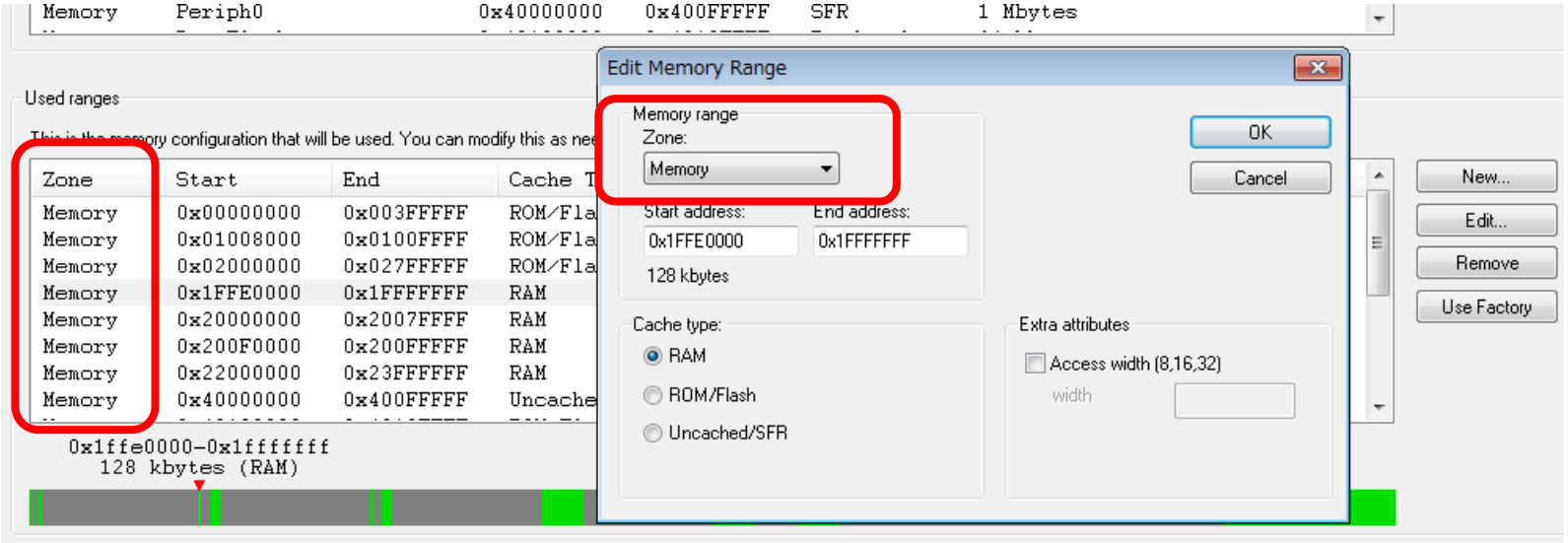
- Uncached/SFR
  A range of this type is completely uncached. All read or write commands from a C-SPY window will access the hardware.

6-5. What is Zone?

For normal memory, the default zone Memory can be used.

Certain I/O registers might require to be accessed as 8, 16, 32, or 64 bits to give correct results.

Memory8/16/32/64



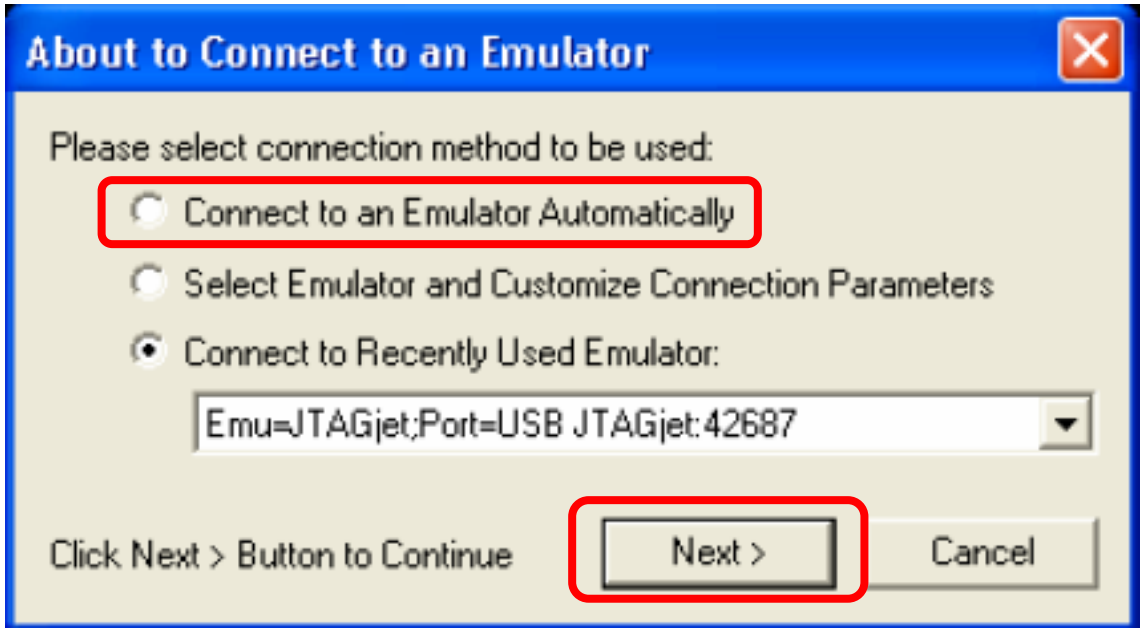
Part 7

- How to use EmuDiag?

- **7-1. Start EmuDiag.exe**
- **7-2. Test USB connection**
- **7-3. Check Target Power**
- **7-4. Test JTAG connection for SWD**
- **7.5 Test JTAG connection for JTAG**

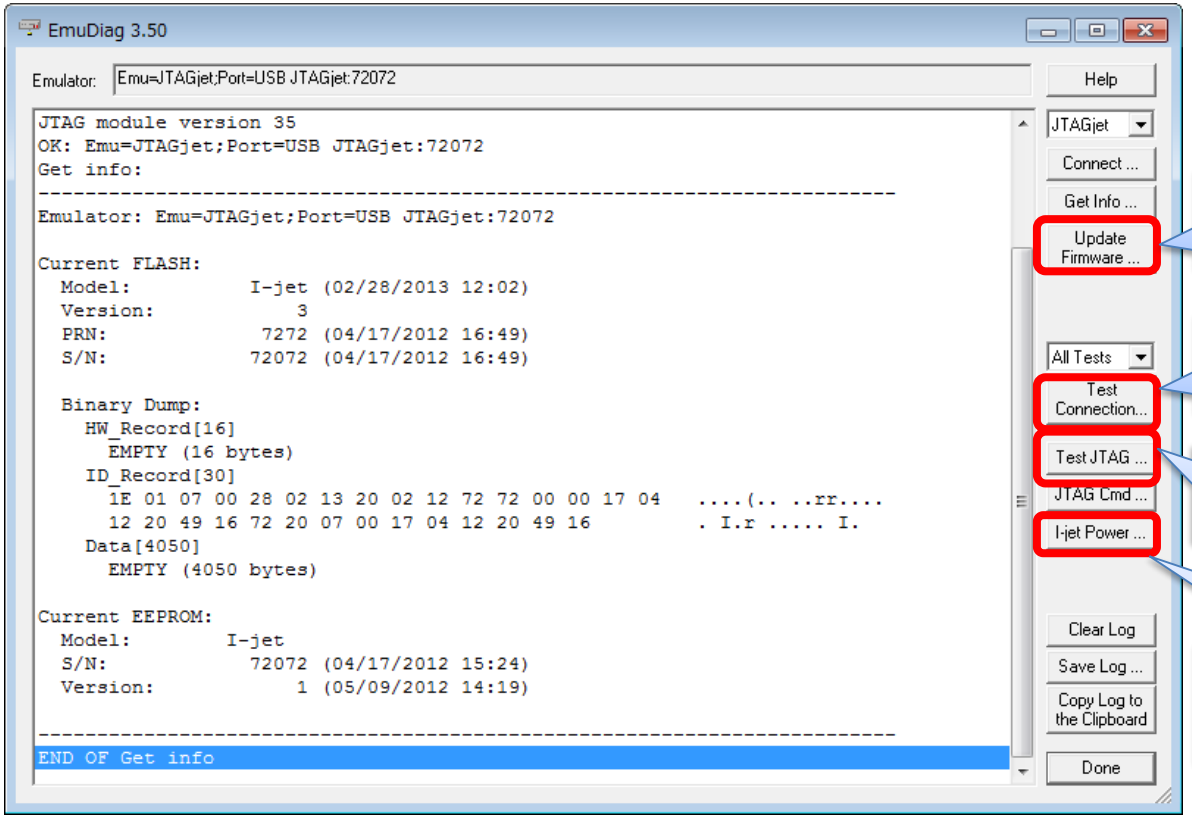
7-1. Start EmuDiag.exe

start “EmuDiag.exe” in \arm\bin\jet which is placed the folder where IAR Embedded Workbench for Synergy is installed



If you connect only one I-jet/I-jet-trace to PC,
you just only select [Connect to an Emulator Automatically]

Main Screen

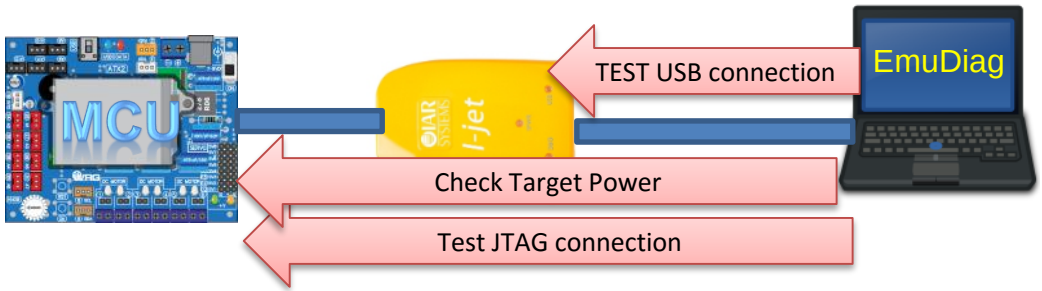


Firmware update

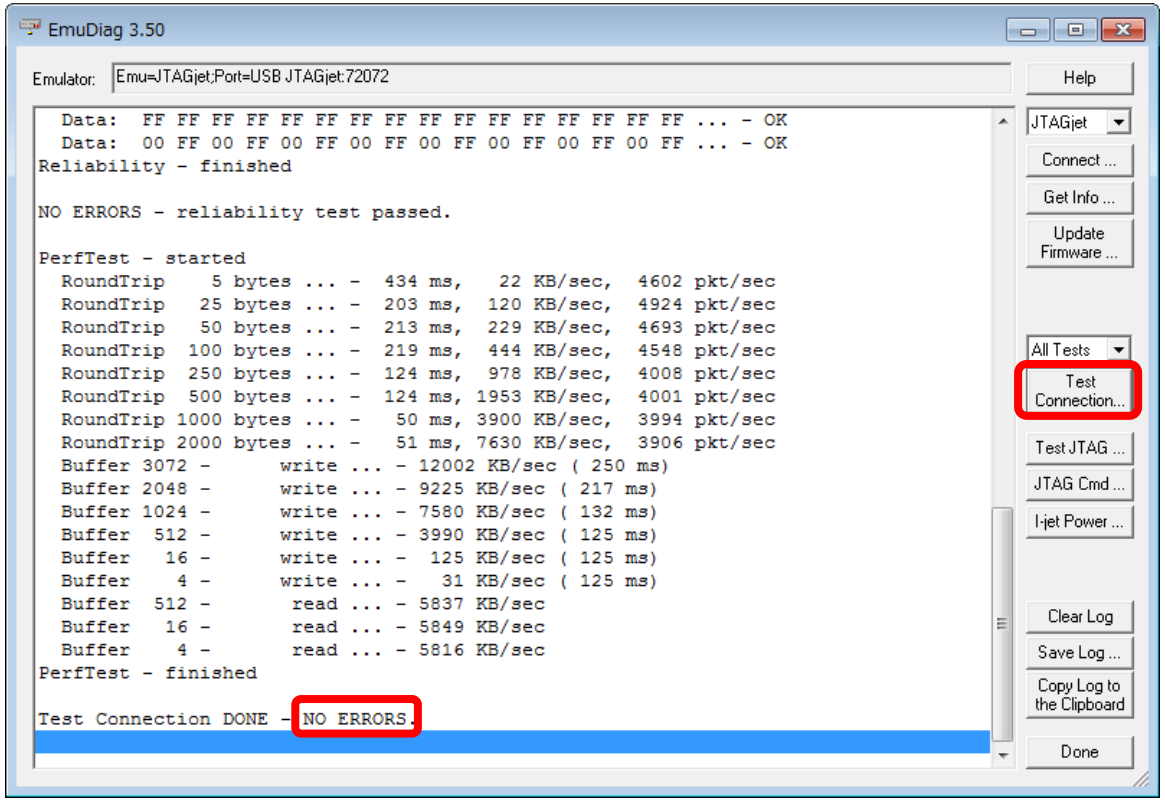
Test USB connection

Test JTAG connection

Check Target Power

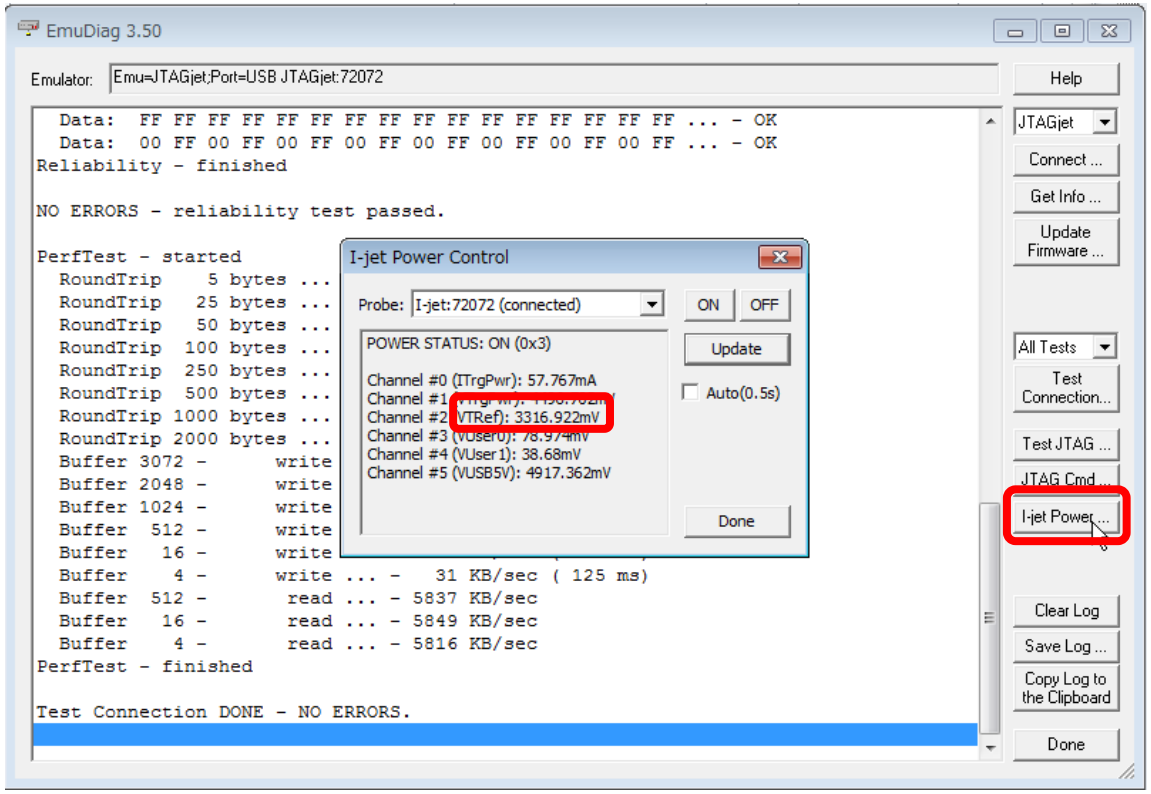


7-2. Test USB connection



If you get message “NO ERRORS”, USB connection is OK.

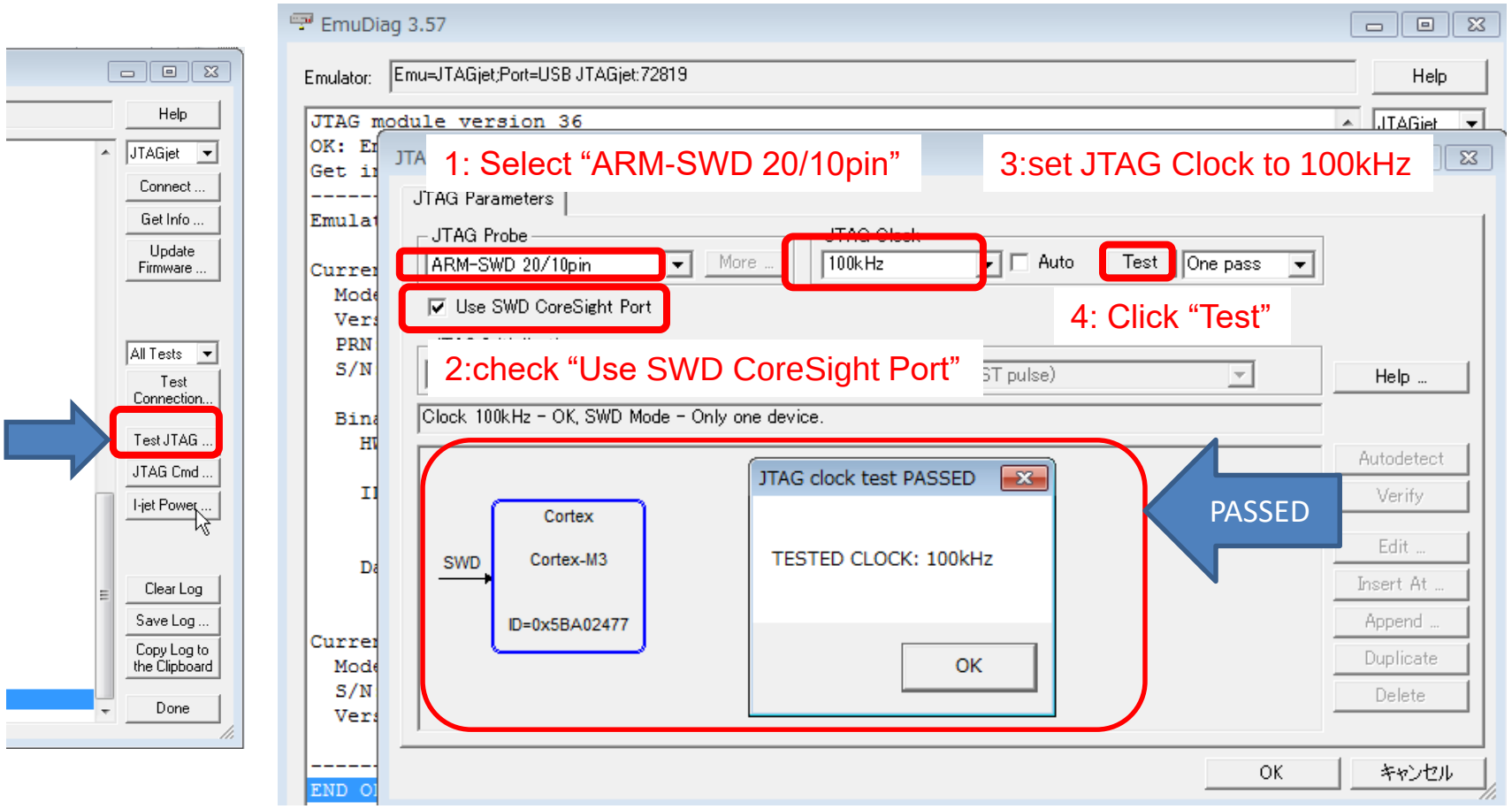
7-3. Check Target Power



If your tareget board has power supply, VTREF shows proper value.

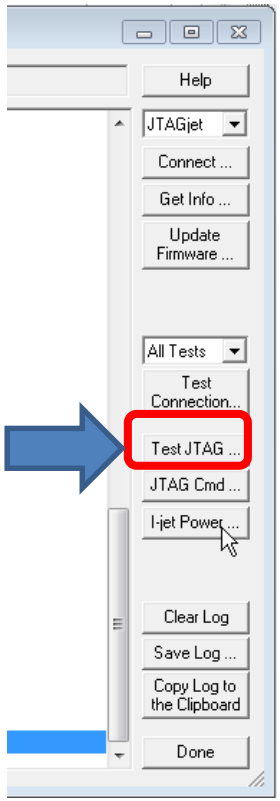
There are two major troubles: 1) no connection to VTREF and 2) power is not supplied to MCU.

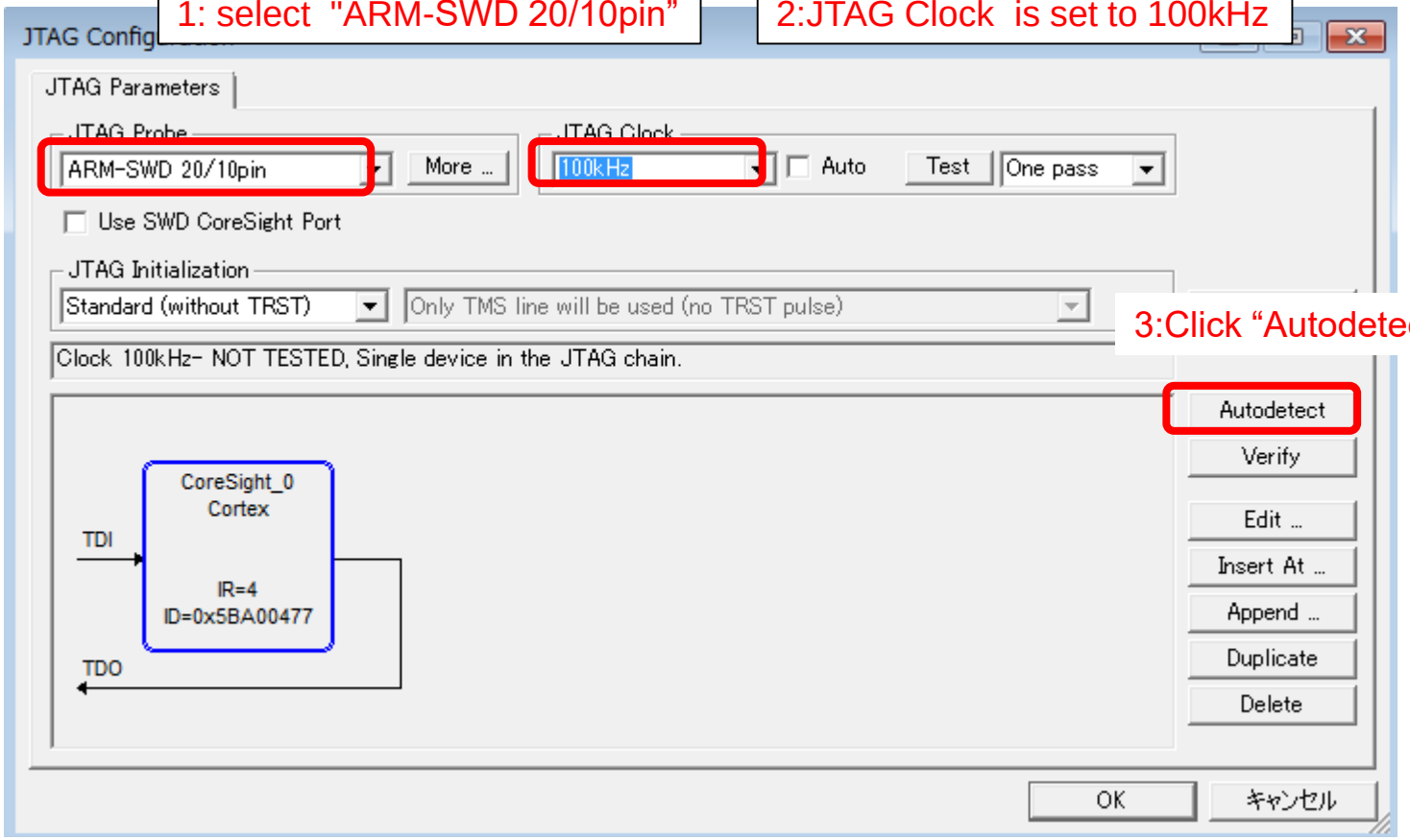
7-4. Test JTAG connection for SWD



If test is passed, try more higher JTAG clock.

7.5 Test JTAG connection for JTAG





If test is passed, try more higher JTAG clock.

Part 8

- Error messages and how to check them

8-1. Fatal error: Probe not found

8-2. Fatal error: Failed connecting to Probe

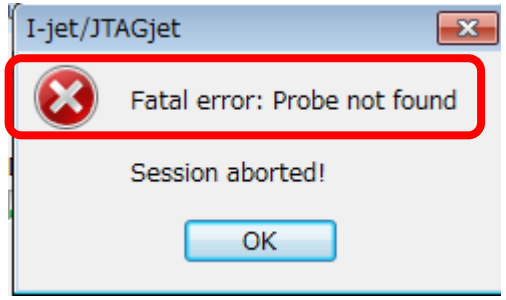
8-3. Warning: I-jet FW is outdated

8-4. program doesn‘t match the expected memory layout

8-5. CPU status NO POWER

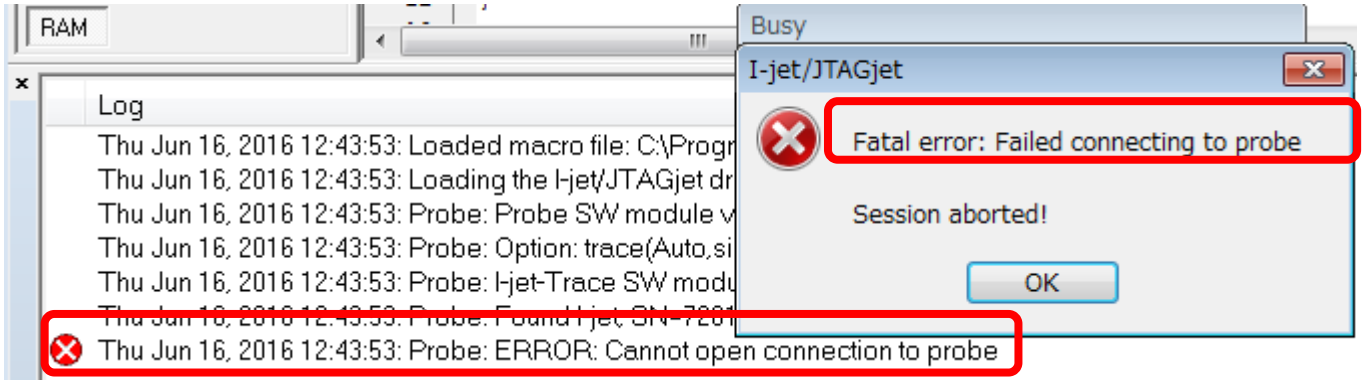
8-6. CPU status failed

8-1. Fatal error: Probe not found



I-jet is not recognized by Windows
[CHECK items]
・Is device driver for I-jet installed?
・Is I-jet connected to PC?

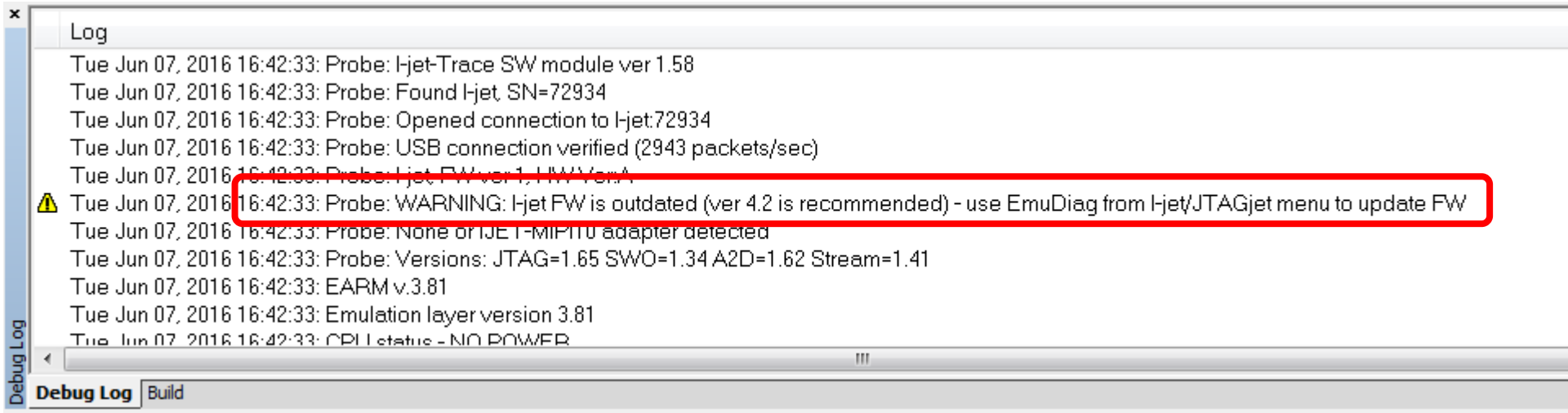
8-2. Fatal error: Failed connecting to Probe



EWARM cannot open connection to I-jet.

・Has Other EWARM or Other Emudiag used I-jet?

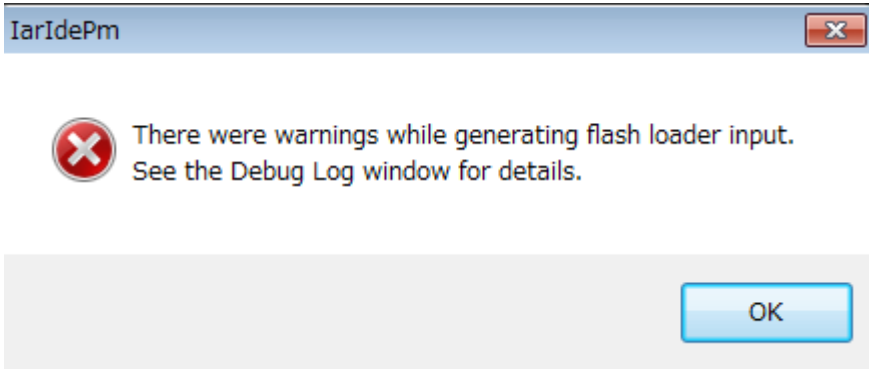
8-3. Warning: I-jet FW is outdated



Firmware of I-jet is outdated.
In the folder where EW for Synergy is installed, there are new firmware.
Updating firmatware is recommended through EmuDiag.

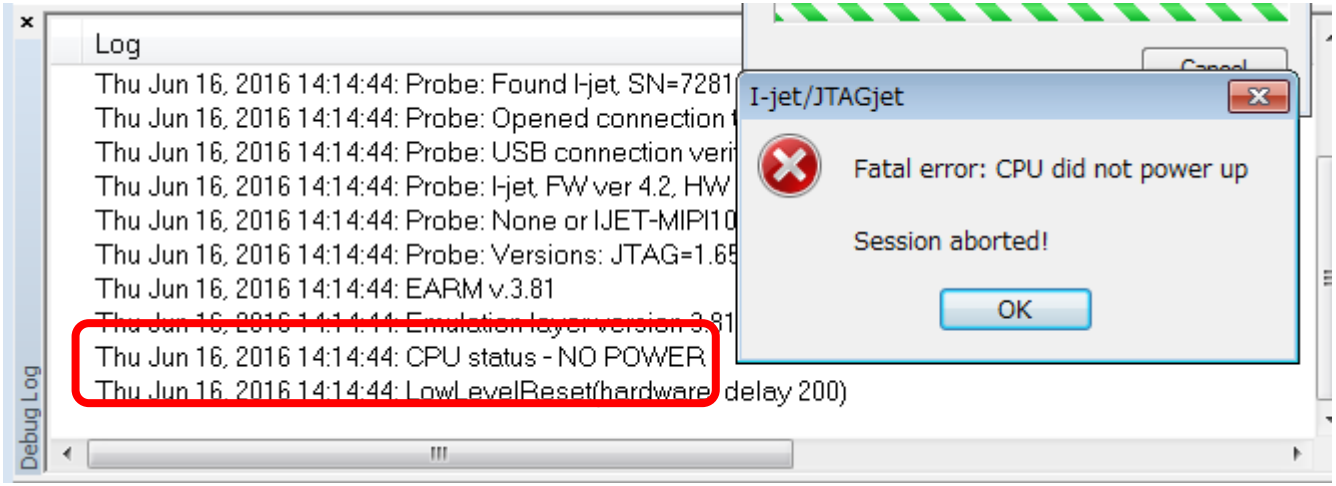
8-4. program doesn‘t match the expected memory layout

Thu Jun 16, 2016 13:00:17: Flash download warning: 4 out of 4 bytes from data record CODE:[0x30000000,0x30000003] will not be flashed
Thu Jun 16, 2016 13:00:17: There were warnings while generating flash loader input.
See the Debug Log window for details.
…
Thu Jun 16, 2016 13:01:07: The downloaded program doesn't seem to match the expected memory layout of the target system:
Thu Jun 16, 2016 13:01:07: Some C variables are placed outside known memory areas:
Thu Jun 16, 2016 13:01:07: ggg @ 0x30000000, int
Thu Jun 16, 2016 13:01:07: Memory is specified as follows:
Thu Jun 16, 2016 13:01:07: 0x00000000 - 0x003FFFFF ROM/Flash
Thu Jun 16, 2016 13:01:07: 0x01008000 - 0x0100FFFF ROM/Flash
Thu Jun 16, 2016 13:01:07: 0x02000000 - 0x027FFFFF ROM/Flash
Thu Jun 16, 2016 13:01:07: 0x1FFE0000 - 0x1FFFFFFF RAM
Thu Jun 16, 2016 13:01:07: 0x20000000 - 0x2007FFFF RAM
Thu Jun 16, 2016 13:01:07: 0x200F0000 - 0x200FFFFF RAM
Thu Jun 16, 2016 13:01:07: 0x22000000 - 0x23FFFFFF RAM
Thu Jun 16, 2016 13:01:07: 0x40000000 - 0x400FFFFF Uncached/SFR
…



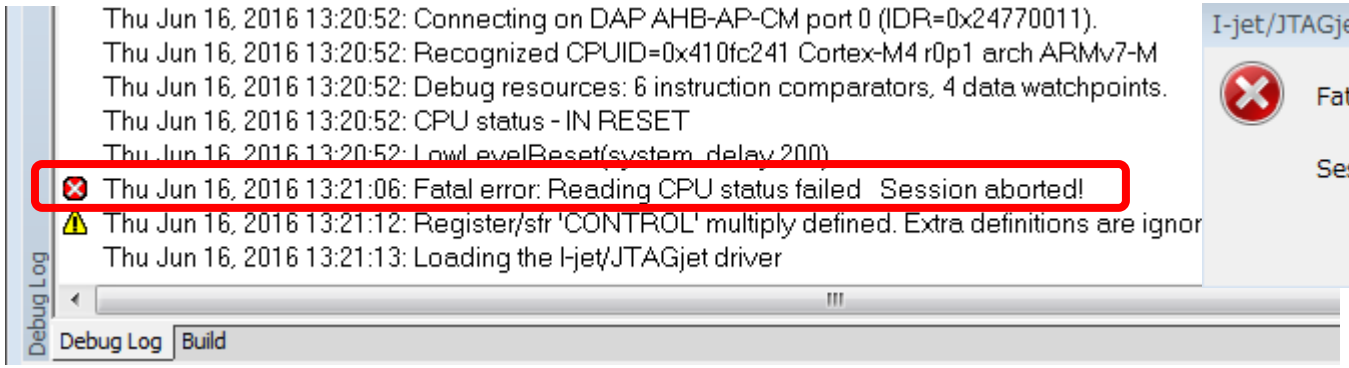
Program has variables/functions out side of memory configuration.
 -> If external memory is used, memory configuration should be customized.
 -> If memory configuration is correct, variables/functions are placed in wrong area.

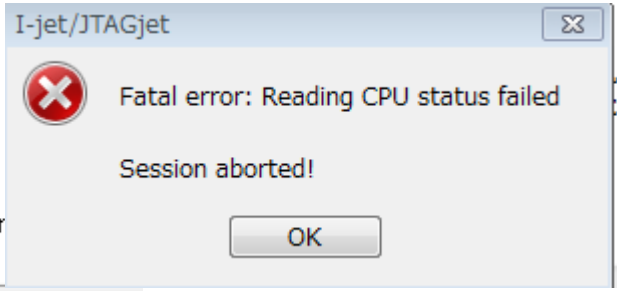
8-5. CPU status NO POWER



Check Power supply
Check VTRef signal is connected to reference voltage.

8-6. CPU status failed





JTAG/SWD connection has trouble

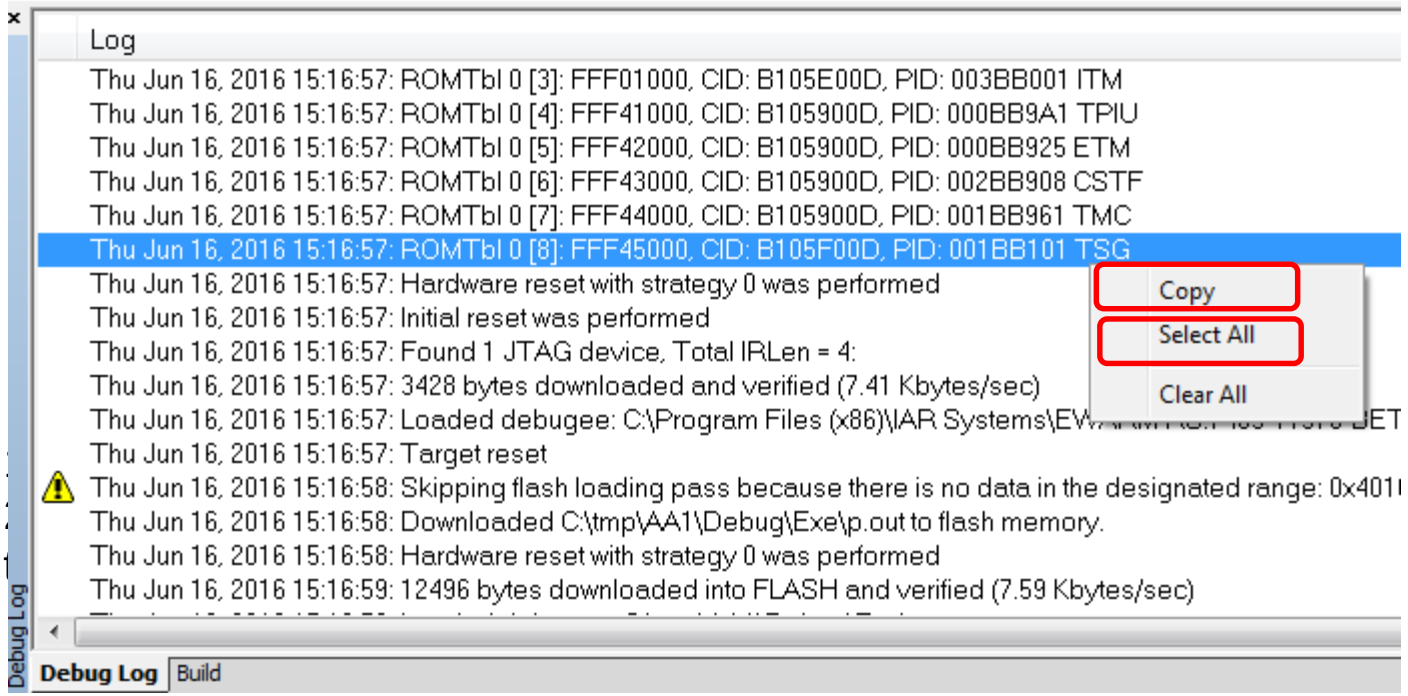
- Do you select right Reset Strartegy?
- Do all JTAG or SWD signals are connected to ICE probe?
- Do you select JTAG or SWD correctly?

Part 9

- How to generate log files?

How to generate LOG information(1)

a. Debug Log

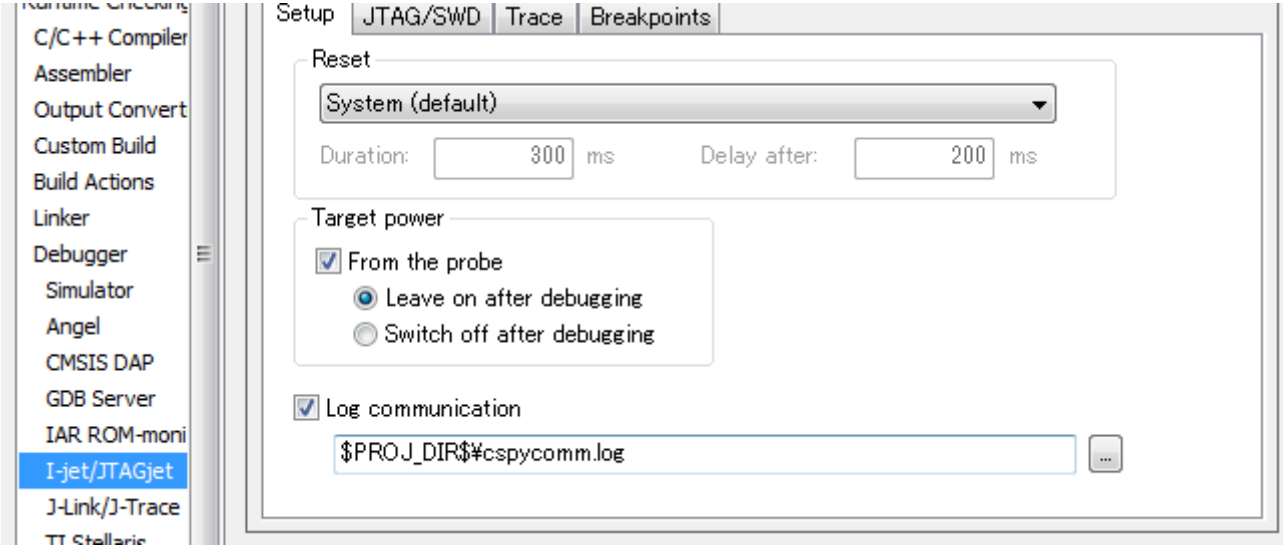


In Debug Log, right click.
1)Select All, 2)Copy, then paste it to text-editor.

How to generate LOG information(2)

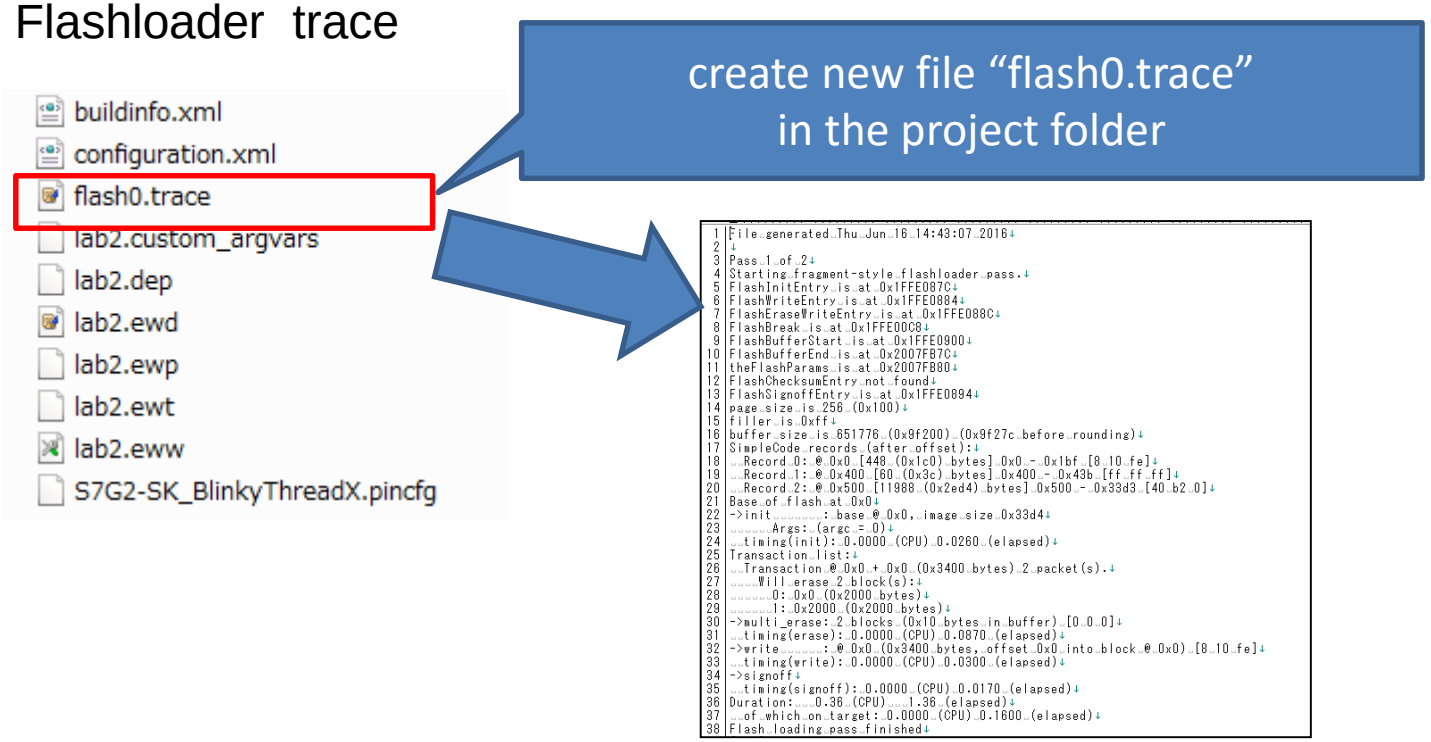
b) log commuincation

[I-jet/JTAGjet]-[Setup]-Enable [Log communication]
Default output file is stored in the project directory ($PROJ_DIR$), the directory where the active project file (ewp) resides



How to generate log information(3)

c. Flashloader trace



To enable trace output, simply create an empty file named flash0.trace in the project directory ($PROJ_DIR$), the directory where the active project file (ewp) resides.